APPENDIX C
TRANSISTOR-TRANSISTOR LOGIC

The line of circuits called transistor-transistor logic (TTL) is now the most widely used because of the high speed of TTL circuits. The characteristic which distinguishes TTL circuits from other circuit lines is a multiple-emitter transistor at the input circuit. The schematic diagram for this kind of transistor is shown as $T1$ in Fig. C.1(a). The multiple-emitter transistor simply has a larger than normal collector area and several base-emitter junctions. The two-emitter transistor in Fig. C.1(a) functions as the two-transistor circuit because the two-emitter transistor is effectively two transistors with a common collector and base. Figure C.1(b) and (c) shows the TTL input circuit in separate transistor and multiple-emitter transistor form. The transistors, $T1A$, $T1B$, and $T1C$ are combined to form a single multiple-emitter transistor $T1$ in Fig. C.1(c). This circuit operates as follows. If one of three inputs X, Y, and Z is at 0 V, current will flow through $R1$ and the base-emitter junction of $T1$ to the input. This will hold the base of $T1$ at about 0.5 V. The base collector of $T1$ and the base emitter of $T2$ form two junctions in series with resistor $R3$ to ground, and so the base of $T2$ will not be positive more than 0.2 V, which is insufficient to turn on $T2$. Little (leakage only) current will flow in the collector circuit of $T1$, and $T2$ will be off. As a result, no current will flow through resistors $R2$ and $R3$, and the emitter of $T2$ will be at ground and the collector at $+5$ V.

If all three inputs are at a level of $+3.5$ V (the 1 level), then current will flow through $R1$ and the base-collector junction of $T1$ (which is forward-biased) into the base of $T2$, turning it on. Current will flow through $R1$ and $R2$ until the transistor $T2$ is saturated with its emitter and collector both at about 2.5 V. At this time, the three emitter-base junctions of the multiple-emitter transistor will be reverse-biased.
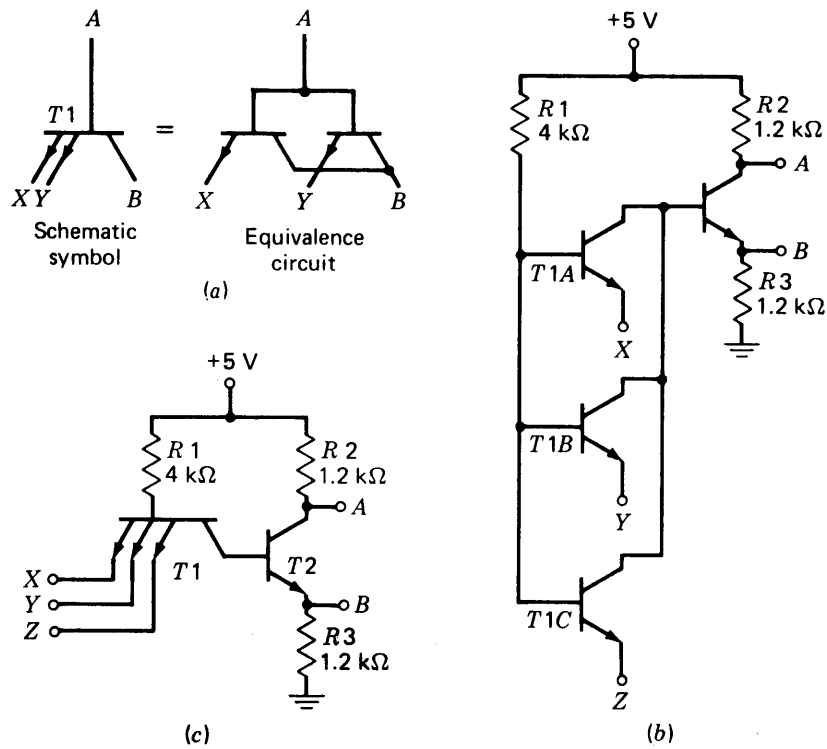
A

T1

XY B

Schematic
symbol

=

X Y B

Equivalence
circuit

(a)

+5 V

R 1
4 kΩ

R 2
1.2 kΩ

A

X o—
Y o—
Z o—

T1

T2

B

R3
1.2 kΩ

(c)

+5 V

R 1
4 kΩ

R 2
1.2 kΩ

A

T1A

B

R 3
1.2 kΩ

X

T1B

Y

T1C

Z

(b)

FIGURE C.1

TTL gate circuit. (a)
Schematic symbol
and equivalent cir-
cuit. (b) Discrete ver-
sion of TTL gate.
(c) Multiple-emitter
TTL gate.

The two outputs from the collector and emitter of $T2$ operate as scissors which close when $T2$ is on and open when $T2$ is off. That is, the emitter and collector of $T2$ will be at about the same voltage (closed) when $T2$ is on, and the emitter will be at ground and the collector at $+5$ V when $T2$ is off (open scissors).

Notice that $T2$ is on when the three inputs are high (1s) and off when any one of the three inputs is low (a 0). So the circuit operation is basically that of a NAND gate. Logic levels for TTL are that 0 to 0.2 V represents a 0 and $+2.5$ to $+5$ V represents a 1.

A complete TTL NAND gate is shown in Fig. C.2. This is a *second-generation* TTL circuit and is typical of the circuits offered by the major TTL manufacturers in their medium-speed lines.

Let us examine the operation of the circuit in Fig. C.2 by assuming that input Y is at $+3.5$ V and X is at 0 V. Therefore $T1$ has its base-emitter junction connected to Y reversed-biased, and the full current from $R1$ flows through the base-emitter junction connected to X. At this time, (1) $T2$ will be off; (2) $T4$ will be off because with no current through $R4$ its base will be at essentially ground; (3) $T3$ and $T5$ will be turned on by current flowing through $R2$. The transistors $T5$ and $T3$ are connected in what is called a *Darlington configuration* which gives large current gain. As a result, little current will be required through $R2$ to turn on $T3$, and the output will be at $+5$ V minus the base-emitter drops for $T5$ and $T3$, or about $+4$ V.

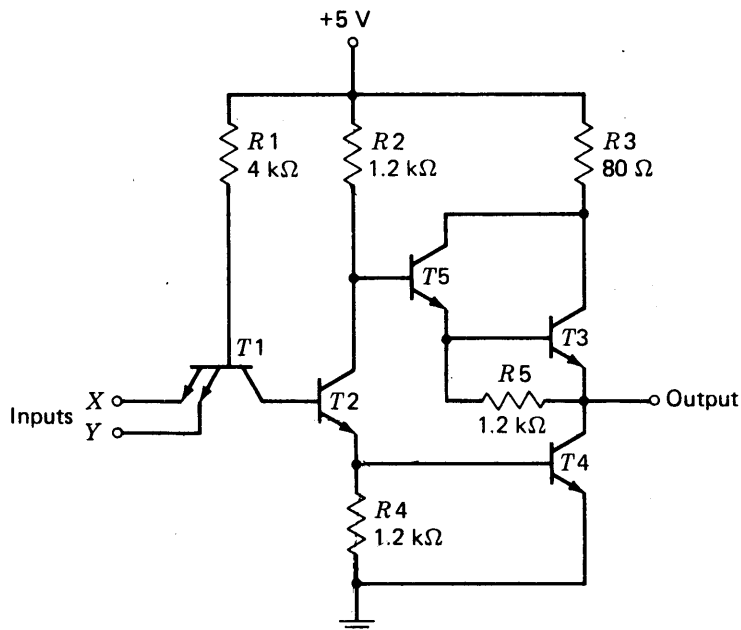Let us consider that the input voltage at X is slowly raised positive. As a

FIGURE C.2

Classic TTL NAND
gate.

result, the collector of $T1$ goes positive, and $T2$ begins to conduct. As the emitter of $T2$ becomes more and more positive, $T4$ begins to conduct, and as the collector of $T2$ becomse more and more negative, the $T5$ to $T3$ combination begins to turn off. Finally $T2$ will saturate and $T4$ will be saturated, and therefore about $+0.5$ V or less.

The circuit in Fig. C.2 will have about 4-ns turn-on delays and 7-ns turn-off delays and a power dissipation of about 10 mW.

The reason for the high speeds lies in the all-transistor construction of the TTL and in the fact that the final stage drives current in both directions. The standard transistor inverter has an output which is "driven down" by the turning on of the output transistor. When the transistor is turned off, however, the rising edge is formed by the resistor at the circuit's output supplying current to all the stray capacity in this circuit and any circuits connected to the output. Therefore the rise time is exponential. With TTL's two-transistor output (the circuit is called a *totem pole*), the rising edge is "driven up" by the upper transistor turning on and the lower transistor turning off. This gives a sharp edge, and the falling edge is similarly sharp.

In many aerospace, military, and industrial applications, it is desirable to have a much lower power dissipation. If the resistor values in the basic circuit design shown in Fig. C.2 are raised, the circuit will consume far lower power, and circuit manufacturers offer low-power TTL circuits. Typical resistor values are $R1 = 40$, $R2 = 20$, $R3 = 500$, $R4 = 12$, and $R5 = 5$ kΩ. Naturally there will be a decrease in speed, but low-power gates are still capable of 23-ns delays at only 1-mW power dissipation.

There is a famous problem with TTL circuits which can be illustrated by

using Fig. C.2. When TTL circuits are switched, they generate large "spikes" on their outputs, and interconnections must be carefully watched to prevent ringing or even circuit damage. Sometimes, capacitors are even placed across the +5 V to ground power supply on each circuit container to prevent spikes in the power-supply voltage.

The problem develops because it is possible for both T3 and T4 to be on simultaneously when the circuit is switching. For instance, if the output is switching from a 0 to a 1 level, then T4 must go off and T3 must go on. But if T3 goes on before T4 is completely off, then both transistors will be on simultaneously, almost short-circuiting the +5 V to ground.

The TTL current spike problem has plagued the TTL family and is clearly in evidence in the circuit of Fig. C.2. While T3 and T4 can both be on during turn-on and turn-off, the turn-off case is usually worse since the storage time of T4 causes both transistors to be on for a greater time. Turn-on current spiking may be lowered by increasing the ratio of R2 to R4. In this way the collector of T2 reaches a lower voltage before T4 begins to conduct. There is a tradeoff involved, however, since increasing R2 decreases the on drive for T4, decreasing its turn-on time. The increased value of R2 also results in decreased noise immunity. So far, no perfect answer to current spiking has been found.

Although the standard TTL circuits are fast, there is always a desire to speed up circuit lines. To increase still further the speeds of TTL, a basic problem must be dealt with. When a transistor is saturated and must be turned off, before the transistor begins to go off there is a delay (caused by the minority carriers) called the *storage time delay*. This is shown in Fig. C.3(a) where a transistor inverted is turned off from saturation. While this delay is on the order of nanoseconds, it is

FIGURE C.3

Schottky clamped transistor. (a) Storage delay. (b) Schottky diode and transistor.

(a)

(b)
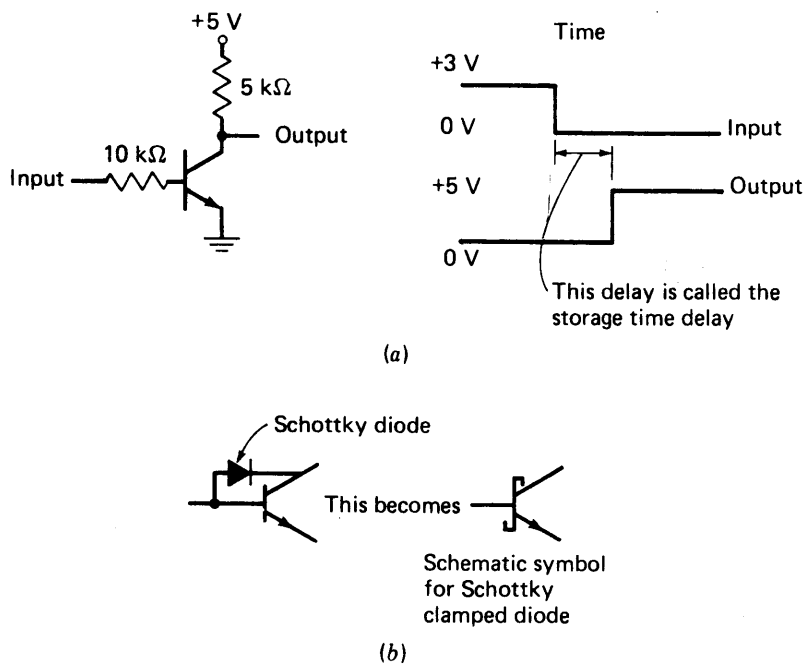
still significant since several of the TTL circuit transistors become saturated at various times.[1]

To alleviate this problem, the fastest TTL circuits use a diode clamp between base and collector. This is shown in Fig. C.3(b). The diode used is not a conventional diode, however, but a special diode (called a *Schottky diode*) formed by the junction of a metal and a semiconductor.

The Schottky diode is faster than conventional diodes because electrons which have crossed the junction and entered the metal when current is flowing are not distinguishable from the conduction electrons of the metal. Since these electrons are majority carriers, there is no delay associated with minority carrier recombination as in semiconductor diodes. As a result, reverse recovery times from Schottky diodes are generally in the low picosecond range. Further, because of the choice of materials (aluminum or platinum silicides), the forward drop of the Schottky diode is less than for a conventional diode.

The transistor with a Schottky diode connected from base to collector will switch faster because the transistor is not allowed to saturate. The minority carrier storage time normally associated with the transistor's operation when coming out of saturation is avoided and the circuit can operate faster.

When a transistor is fabricated with a Schottky diode connected from base to collector, the combination is given a special schematic diagram symbol as shown in Fig. C.3(b).

The use of Schottky clamped transistors has resulted in a series of high-speed TTL circuits with delays on the order of 1 ns (rise and fall times are on the order of 2 ns). Figure C.4(b) shows a typical circuit. Notice that the transistors which normally become saturated at some time are now Schottky clamped transistors, and so storage delays are reduced. The operation of this circuit is essentially the same as that of Fig. C.2 except that the transistors do not saturate.

The diodes connected to ground at the inputs dampen negative spikes and negative-going signals which may occur during ringing. These circuits must be carefully interconnected, however. Wire or printed-circuit connections of more than 8 in. in length should be treated with respect and terminated according to the rules given by the circuits' manufacturers.

Table C.1 gives some of the characteristics of several TTL lines. Notice that speed is associated with power consumption.

TTL circuits are also available in MSI. The MSI seven-segment decoder and BCD counters in Chap 4. were TTL. A simplified TTL gate is used internally for such MSI circuits, and this gate is shown in Fig. C.4(a).

Manufacturers make a special TTL gate which can be connected in a wired-AND circuit. Figure C.5(a) shows the basic circuit. The inputs are ANDed by the multiple-emitter input transistor and inverted by the output transistor. The output transistor has no resistor to +5, however, and so the circuit is not completed and an external resisitor must be supplied. The advantage of the circuit is that if two or more of these circuits have their outputs connected, they form a NAND-to-wired-AND configuration as in Fig. C.5(b).

Figure C.5(b) also shows that a resistor must be connected to +5 from the

---

[1]Gold doping is often used to reduce minority carrier storage times in switching transistors.
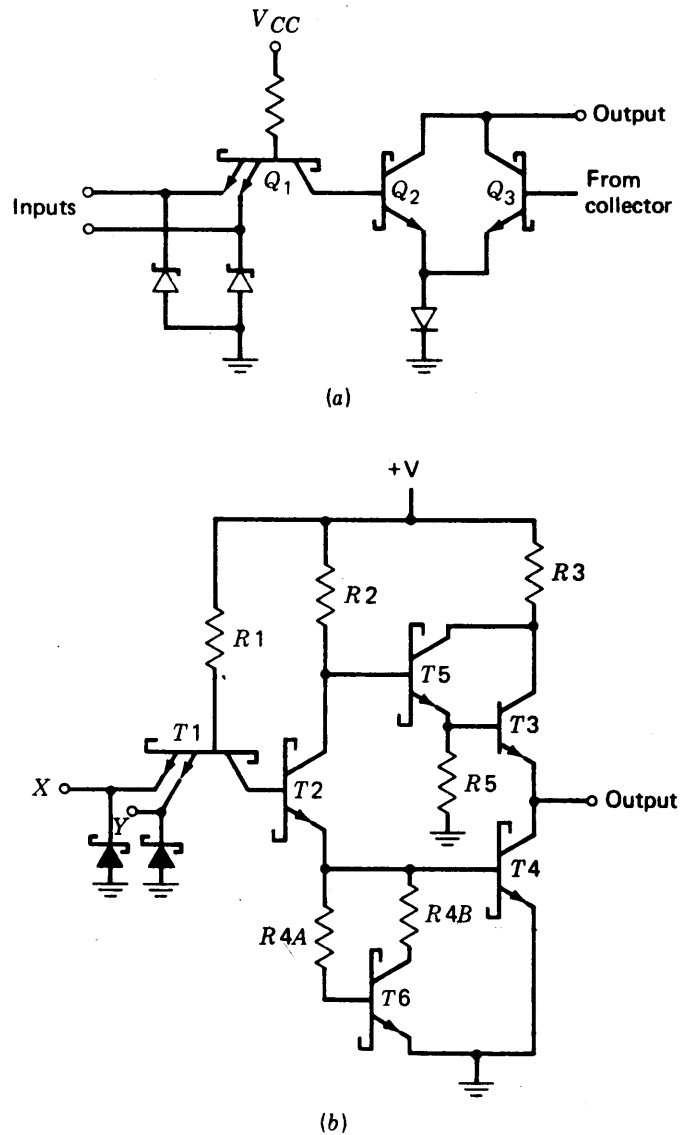
(a)

(b)

FIGURE C.4

(a) Schottky MSI circuit. (b) Schottky clamped TTL gate.

wired-AND output, but only a single resistor is required. Generally, this resistor is not shown on block diagrams, but it is included in Fig. C.5(b) to show how the circuit is connected. The AND function is performed at the outputs because if any output transistor is on (saturated), it will force all outputs to the 0 level at about 0.2 V.

Several open-collector NAND gates are packaged in a single IC container. Using this gate makes for economical, reasonably fast circuitry, and they are widely used. The gates can also be used to connect to bus wires which are normally high but which are to be forced low to indicate status.

| TABLE C.1 | | | | TTL CHARACTERISTICS |

	VERY HIGH SPEED 74 S (SCHOTTKY CLAMPED)	HIGH SPEED	MEDIUM SPEED 74	LOW SPEED 74 L
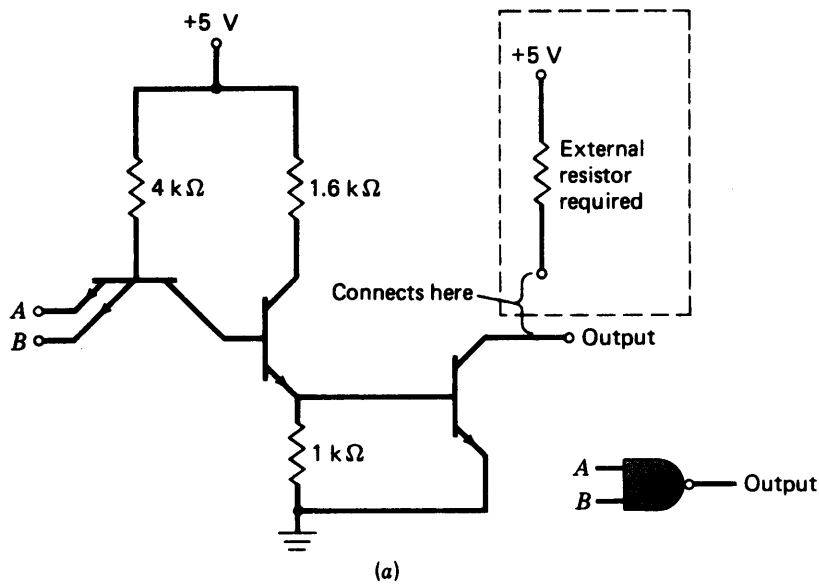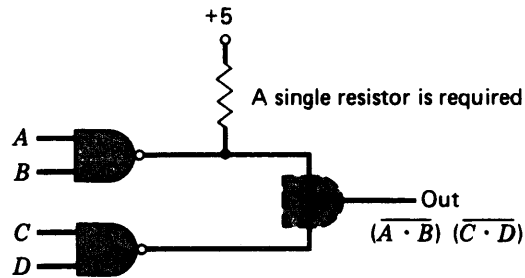
FIGURE C.5

Open collector TTL gate and wired AND connection. (a) Open collector TTL gate. (b) Open collector TTL gates connected in wired-AND configuration.

(a)

(b)

APPENDIX D
EMITTER-COUPLED LOGIC

Emitter-coupled logic (ECL) has several other common names: *current-mode logic* (CML), *current-steering logic,* and *nonsaturating logic.* The last term is the key to this type of circuit. When transistors are operated in a saturated condition, they turn off slowly because of the delay caused by a charge stored in the collector and base region.[1] This delay in turn-off time can be eliminated by operating transistors only in either the active or the off regions. As will be seen, in these circuits current is "steered" rather than having voltages or levels passed around.

The ECL line is the fastest currently available. Manufacturers of ECL have a number of basic circuits, each with different features and drawbacks. ECL has not proved as popular as TTL, primarily because it is more expensive, harder to cool, and more difficult to interconnect and is considered to have less noise immunity (this is debatable). Also, ECL may be faster than is necessary in many applications. On the other hand, the superfast computers use ECL as do a number of the highest speed special-purpose computers.

The basic ECL configuration can be best described by examining a particular inverter. Figure D.1 shows an ECL inverter with an input X. The logic levels in this system are as follows: Binary 0 is represented by -1.55 V and binary 1 by -0.75 V. Notice that this is "positive logic," since, although both levels are negative, the more positive level, -0.75, is the binary 1. Also, notice the small signal difference between 0 and 1.

The circuit's operation is based on a *differential amplifier* consisting of $T4$

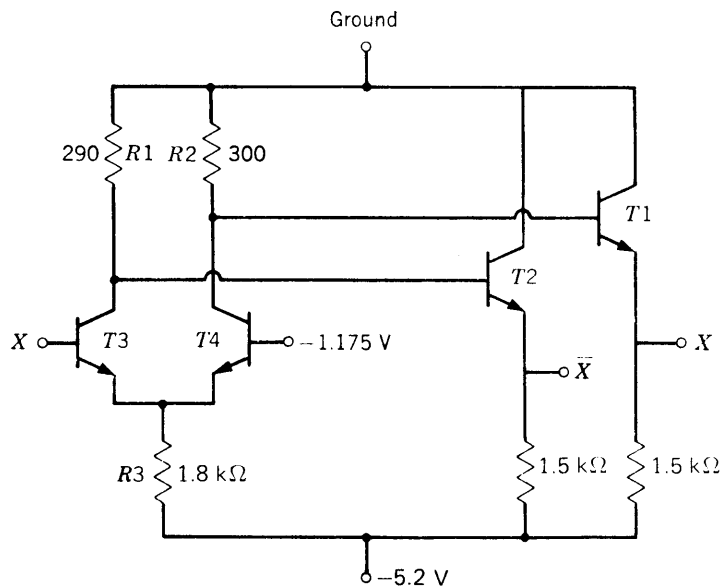[1] This was called the storage delay in the preceding section.

FIGURE D.1

Basic circuit of ECL gate. (*Motorola Corp.*)

and *T*3. When the input to *T*3 is at -1.55 V, *T*3 will be off and current will flow through *R*3 and *R*2. Calculation will indicate a drop of about 0.8 V across *R*2. So figuring a base-emitter drop of 0.75 V for *T*1, we see the *X* output will be at -1.55 V.

Since *T*2 is cut off by the -1.55-V input, very little current will flow through *R*1, and the output $\overline{X}$ will be at the base-emitter drop voltage across *T*2. So the output will be at -0.75 V.

An examination will show that if the input is at -0.75 V, transistor *T*3 will be on, *T*4 will be off, the *X* output will be at -0.75 V, and the $\overline{X}$ output at -1.55 V. (The key to analyzing this circuit is to notice that in a differential amplifier circuit such as the *T*3 to *T*4 form, the current through the resistor *R*3 shared by the two emitters will be almost constant.) Notice that the transistors are never saturated. They are either in their active region or off.

A three-input gate is shown in Fig. D.2. This is a combined NOR and OR gate, as shown by the block diagram, depending on which output connection is used.

As time has passed, several generations of ECL circuits have evolved. In general the circuits have become faster and require more power with each generation. More facilities and more complicated logic per chip are also available in the new lines, including MSI chips. Notice that the circuits in Fig. D.1 require three voltages: ground, -1.175 V, and -5.2 V. Later circuits provide a circuit on each chip to generate the intermediate voltage (in this case, -1.175 V), so that only a single power supply is required.

Figure D.3 shows the four generations Motorola has gone through with their
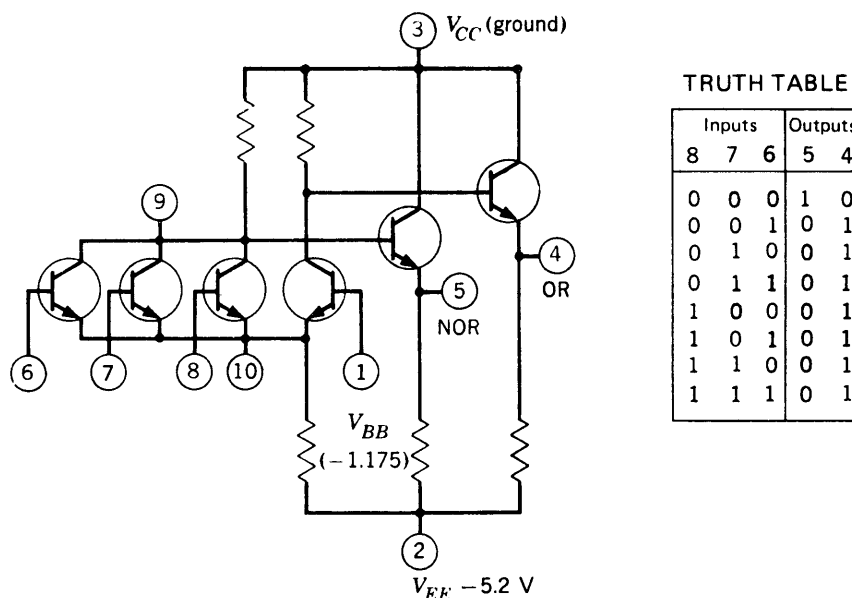
V_{CC} (ground)

TRUTH TABLE

| Inputs			Outputs	
8	7	6	5	4
0	0	0	1	0
0	0	1	0	1
0	1	0	0	1
0	1	1	0	1
1	0	0	0	1
1	0	1	0	1
1	1	0	0	1
1	1	1	0	1

V_{EE} −5.2 V

FIGURE D.2

ECL three-input gate.

ECL which is called Motorola ECL, or MECL, and also Fairchild's 10,000 series. Table D.1 outlines some of the characteristics of these circuits, and the speed versus power and general noise characteristics can be deduced from the table. From Fig. D.3 it is evident which variations were employed as technology advanced. For instance, notice that the circuit to produce the third − 1.175-V bias voltage for the MECL 1 line is not included on the chip, whereas all subsequent lines have this as an internal feature.

Corresponding resistor values differ among MECL lines. This is necessary to achieve the varying speed and power improvements. Of course, speed is not determined by resistor values alone; transistor geometries, while not shown on a schematic, are a major factor. The transistor geometries in conjunction with the resistor values provide the speed and power characteristics of the different families.

Notice also that Fairchild 10,000 and MECL III gates are supplied with base pull-down resistors (50 kΩ) to each of the input transistors, while the other two families are not. These resistors provide a path for base leakage current to unused input bases, causing them to be well turned off.

A final significant difference between the families is in the output circuits. MECL I circuits normally are supplied with output pull-down resistors on the chip. MECL II circuits can be obtained with or without output resistors. MECL III and Fairchild 10,000 circuits normally have open outputs. The use of on-chip output resistors has both advantages and limitations. An advantage is that fewer external components are required. However, with open outputs the designer can choose both the value and the location of the terminating resistance to meet system requirements. Finally the use of external resistors reduces on-chip heating and power dissipation, allowing more complex LSI and increasing chip life and reliability.
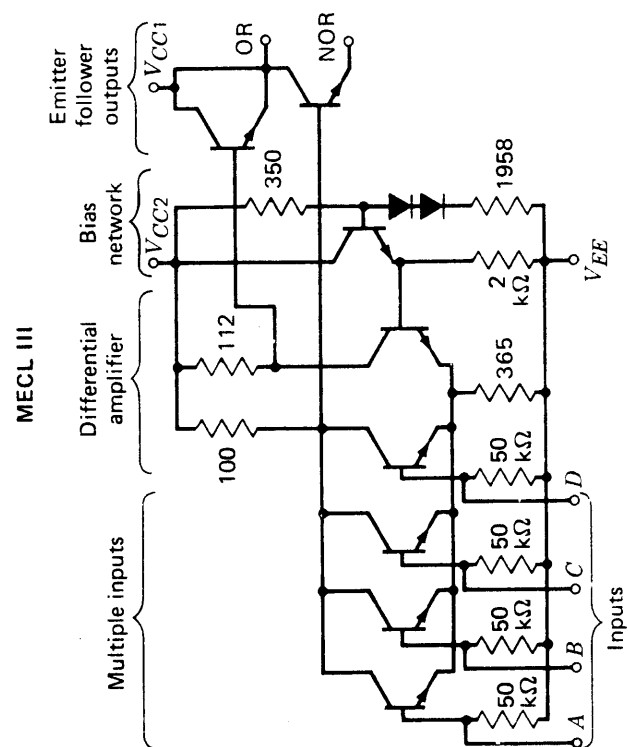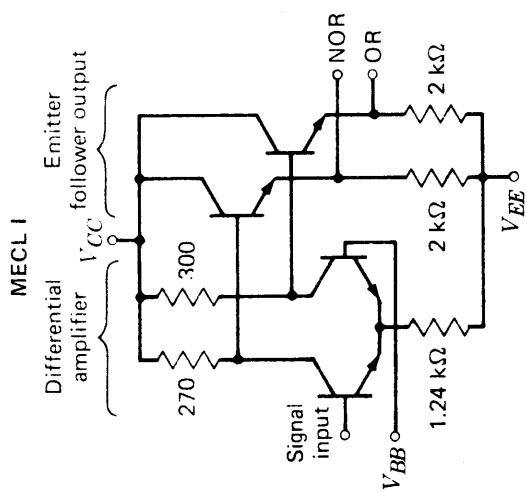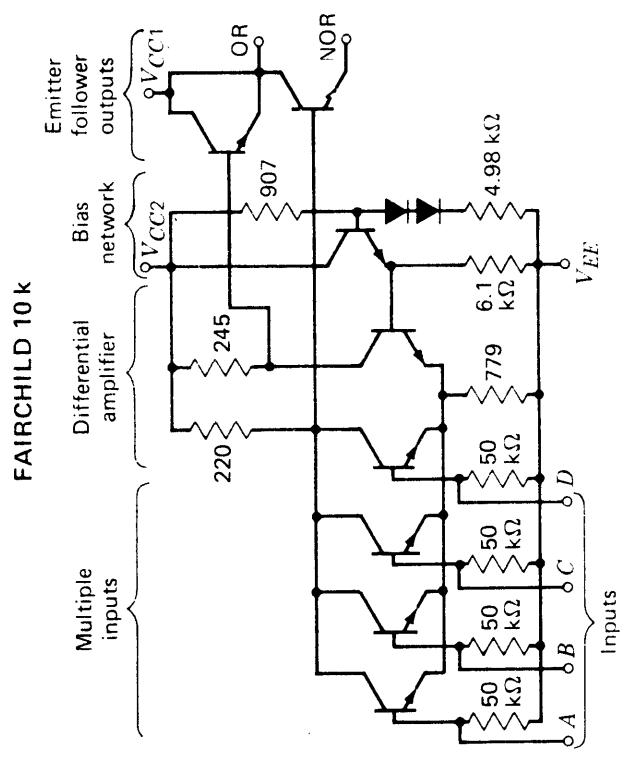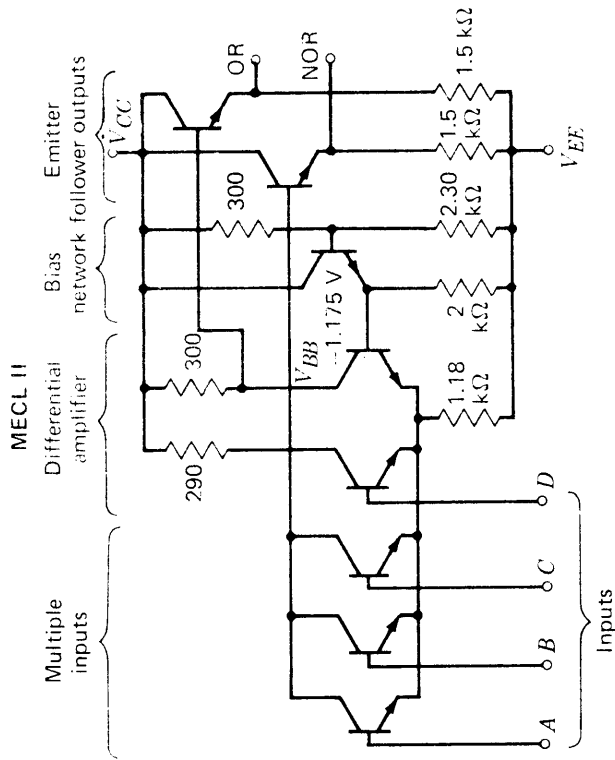
FIGURE D.3

Several generations of ECL circuits.

TABLE D.1			GENERAL CHARACTERISTICS OF ECL CIRCUITS		
			FAIRCHILD		
FEATURE	MECL I	MECL II	10k SERIES	100K SERIES	MECL III
Gate propagation delay, ns	8	4	2	0.75	0.75
Gate edge speed, ns	8.5	4	3.5	1.5	0.75
Flip-flop toggle speed (minimum), MHz	30	70	125	500	500
Gate power, mW	31	22	25	65	60
Input pull-down resistors, kΩ	No	No	50	50	2, 50

APPENDIX E
METAL-OXIDE SEMICONDUCTOR CIRCUITS

The circuits described so far are all termed *bipolar circuits* and use "conventional" transistors. For large-scale integration (LSI), quite often another type of transistor, called a *field-effect transistor* (FET), is used. Although the characteristics of these FETs have not proved desirable for some applications (because of their slowness, delicacy, and lack of drive characteristics), the ease of manufacture, small size, and small power dissipation have offset the negative factors and have led to FETs constructed of metal-oxide semiconductor (MOS) as the primary technology for use in large arrays. FETs constructed of MOS are called MOSFETs.

Figure E.1(*a*) shows a cross section of a FET of *p*-channel type. As shown in Fig. E.1(*b*), a substrate of *n*-type (silicon) material is first formed, and two separate low-resistivity *p*-type regions are diffused into this substrate. Then the surface of this structure is covered with an insulating oxide layer. Holes are cut into the oxide, and two metal contacts are made to the two pieces of *p* material, and a thin piece of metal called the *gate* (*G*) is placed over what is called the *channel*.

With no voltages applied, the above structure (refer to Fig. E.1) forms two diodes back to back. And if we attempt to force current from source to drain, the alternate *pn* junction followed by an *np* junction will not permit current flow (in either direction).

The gate is used to cause and control current flow in the following manner. Consider the source to be grounded and the drain connected to a negative voltage through a resistor. Figure E.2 shows this. [The schematic symbol for the FET is shown in Fig. E.1(*d*).] The metal area of the gate and the insulating oxide layer and semiconductor channel form a capacitor, with the metal gate as the top plate
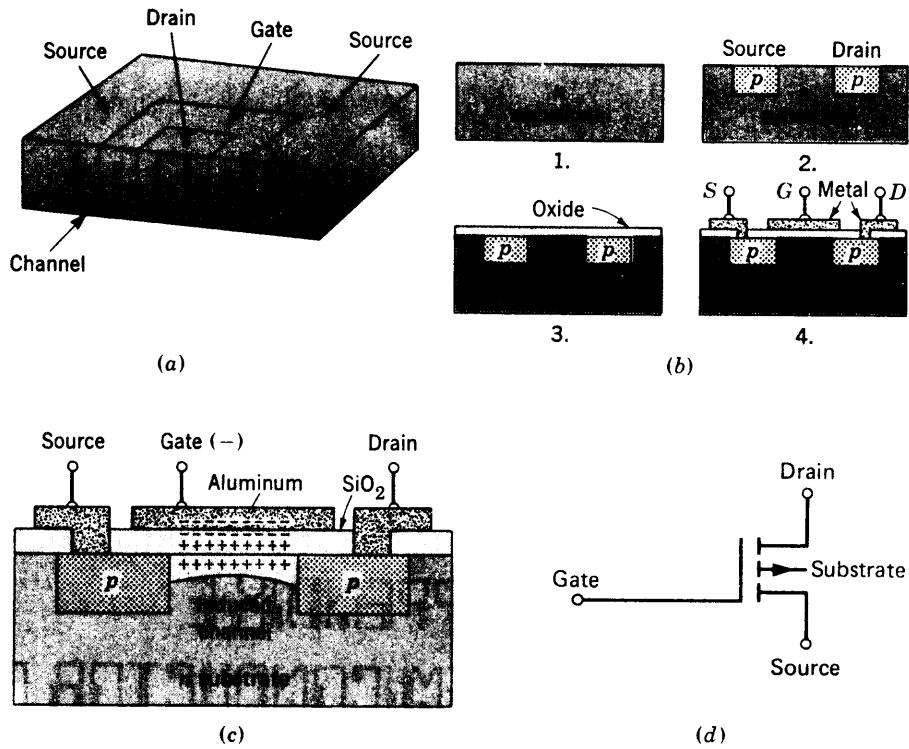
(a)

(b)

(c)

(d)

MOSFET structure.
(a) General configura-
tion. (b) Fabrication
steps. (c) Cross sec-
tion with gate biased
negative. (d) Sche-
matic symbol. (Moto-
rola Corp.)

and the n-material substrate as the lower plate. Making the gate potential negative causes a corresponding positive charge in the n-type semiconductor substrate along the channel, as shown in Fig. E.1(c). Given sufficient negative potential on the gate, the positive charge induced in the channel finally causes this section of material to become p type, and current begins to flow from source to drain—thus the term *current enhancement mode*.

The more negative the gate becomes, the more "p type" the semiconductor channel becomes, and the more current flows. As a result, this type of MOS is also called PMOS.

As a switching circuit, a FET can be used to form an inverter. With a 0, or

FIGURE E.2

Alternative schematic
symbols for MOSFET
resistive element.
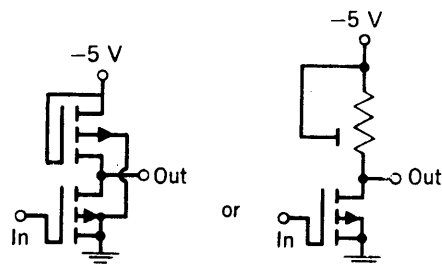
ground, input the output of the circuit shown in Fig. E.2 will have a −5-V output, and with a −2-V or more negative input, the output will go to about 0 V.

Instead of forming actual resistors for these circuits, another FET is used, thus simplifying manufacture. This is shown in Fig. E.2. The FET resistor's gate areas are controlled so that the FET represents a high resistance (perhaps 10 to 100 $k\Omega$) when the gate is at the drain potential. Some manufacturers show this FET by using the regular symbol, and others show the resistor-plus-bar symbol, also seen in the figure.

When a p-type substrate with n doping for the source and drain is used, as in Fig. E.3, then the n-channel transistor is formed as shown. The schematic diagram symbols for the n-channel transistor and an inverter circuit are shown in Fig. E.3(a) and (b). Notice that the circuit uses a positive voltage and behaves similarly to an npn transistor inverter circuit. This type of MOS is called NMOS.

A NOR gate can be formed in NMOS as shown in Fig. E.4(a). The logic levels for this circuit are 0 to 1 V for a binary 0 and $> +1.5$ V for a binary 1. (This is positive logic.) If any of the inputs A, B, or C is a 1, the corresponding FET will conduct, causing the output to go to about +0.8 V or less. If all inputs are at +0.8 V or less, all the FETs will be off and the output will be at +8 V (or more).

Several different gates and flip-flops using NMOS are shown in Fig. E.4. (PMOS is the same except for negative V_{CC} voltages and negative logic.) The high resistances used in these circuits mean low power dissipation. This, combined with the small areas needed to fabricate a FET, makes it possible to fabricate large numbers of circuits on a single small chip.

CMOS logic circuits

A series of circuits using MOSFET transistors called *complementary MOS* (CMOS) was originally developed for the aerospace and oceanographic industries. These circuits have very low power consumption and considerable resistance to noise. They are, however, slow relative to the high-speed logic lines. But large numbers of circuits can be placed on a single chip, the power-supply voltage can vary over a large range, and the circuits are relatively economical to manufacture. The newest CMOS circuits have become relatively fast and are widely used for everything from electronic watches and calculators to microprocessors.

The CMOS circuits are fabricated as illustrated in Fig. E.5(a), which shows that both n- and p-channel transistors can be fabricated on the same substrate.

The simplest form of CMOS integrated circuit consists of one n-channel and one p-channel MOS transistor, with both gate contacts tied together to form the input and both drain contacts tied together to form the output. This circuit is the basic CMOS inverter [Fig. E.5(b)]. When the voltage at the input is near ground level, the gate-to-source voltage of the p-channel transistor approaches the value of the supply voltage $+V$, and the p channel is turned on. A low-resistance path is created between the supply voltage and the output, while a high-resistance path exists between the output and ground, because the n-channel transistor is off. The output voltage will approach that of the supply voltage $+V$. When the input voltage is near $+V$, the p channel turns off and the n channel turns on, causing the output voltage to approach ground.
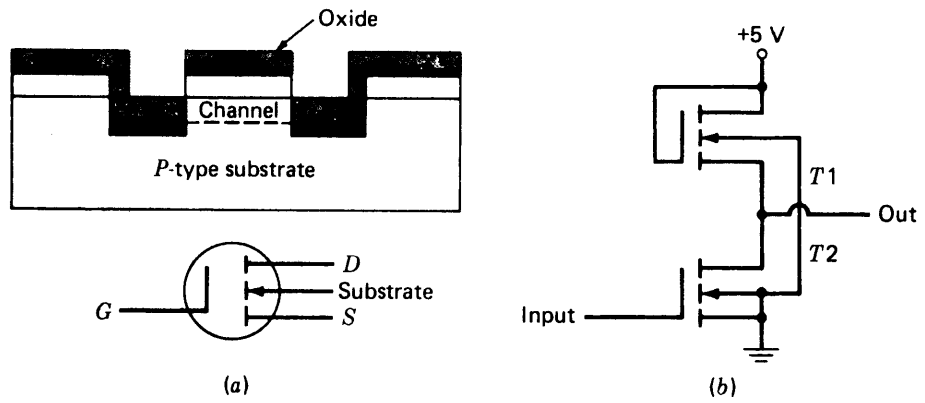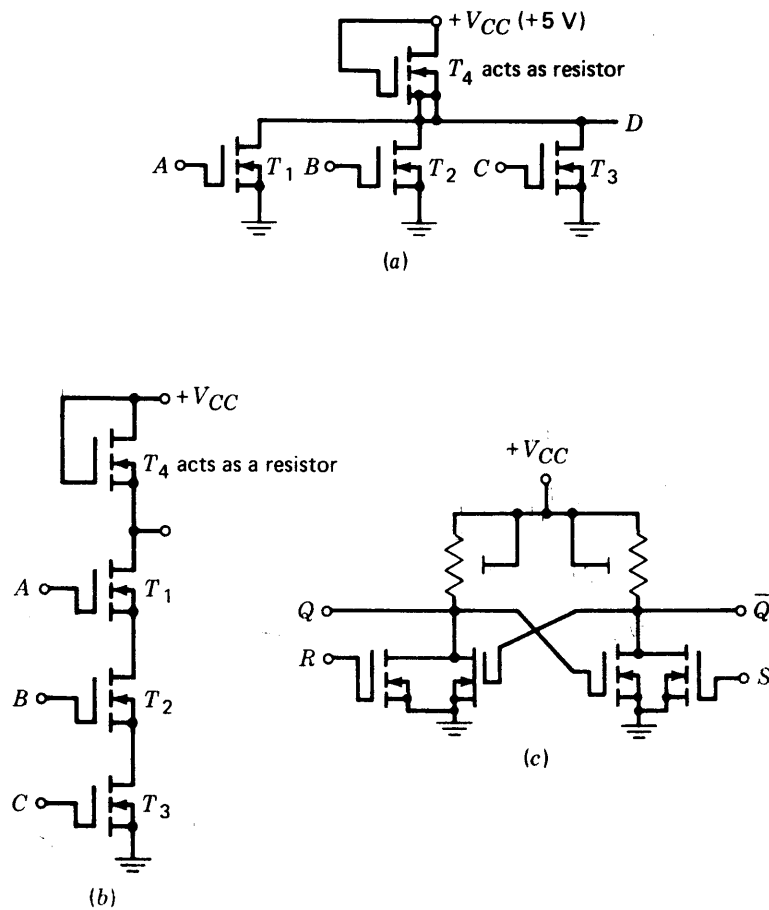
(a)

(b)

FIGURE E.3

(a) n-channel MOS-FET transistor. (b) n-channel inverter.

FIGURE E.4

FET logic circuits.
(a) Three-input NOR gate. (b) Three-input NAND gate. (c) RS flip-flop.

(a)

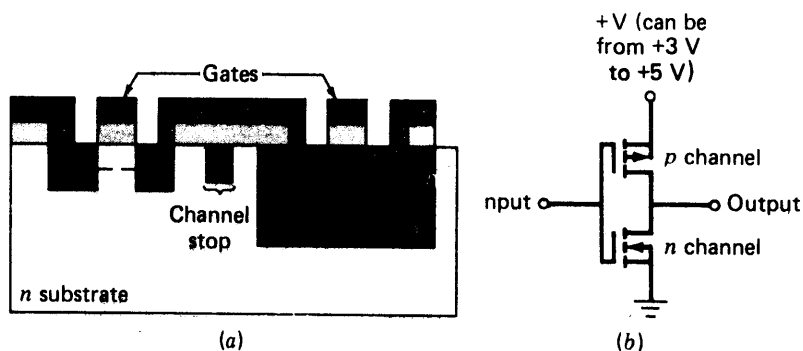(b)

(c)

(a)   (b)

FIGURE E.5

CMOS inverter.
(a) CMOS elements.
(b) Circuit that is the basic CMOS inverter.

Notice that in either state the circuit's power consumption is extremely low because one transistor is always off and because n- and p-channel transistors exhibit very high resistance when off, permitting very low leakage current to flow through the transistor which is in the off condition.

Wnen conventional metal- and silicon-gate technologies are used, protective channel stops are provided to minimize leakage current between separate transistors, as shown in Fig. E.5(a). All p-channel devices must be surrounded by a continuous n-channel stop, which can also act as a conducting path for the external power supply to appropriate locations. Similarly, p-channel stops surround all n-channel devices and provide a conducting path between those n-channel devices which are electrically connected to the lowest potential and the external ground contact.

A two-input NOR gate can be constructed as shown in Fig. E.6. Each additional input requires an additional p- and n-channel pair of MOS transistors.

Table E.1 gives some details of CMOS operation versus other circuit lines. Notice the low power consumption (nanowatts when they are not being switched), competitive speeds, and noise protection.
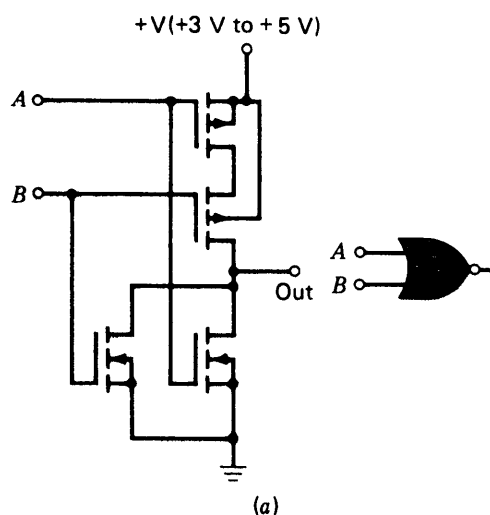
FIGURE E.6

CMOS NOR gate.

(a)

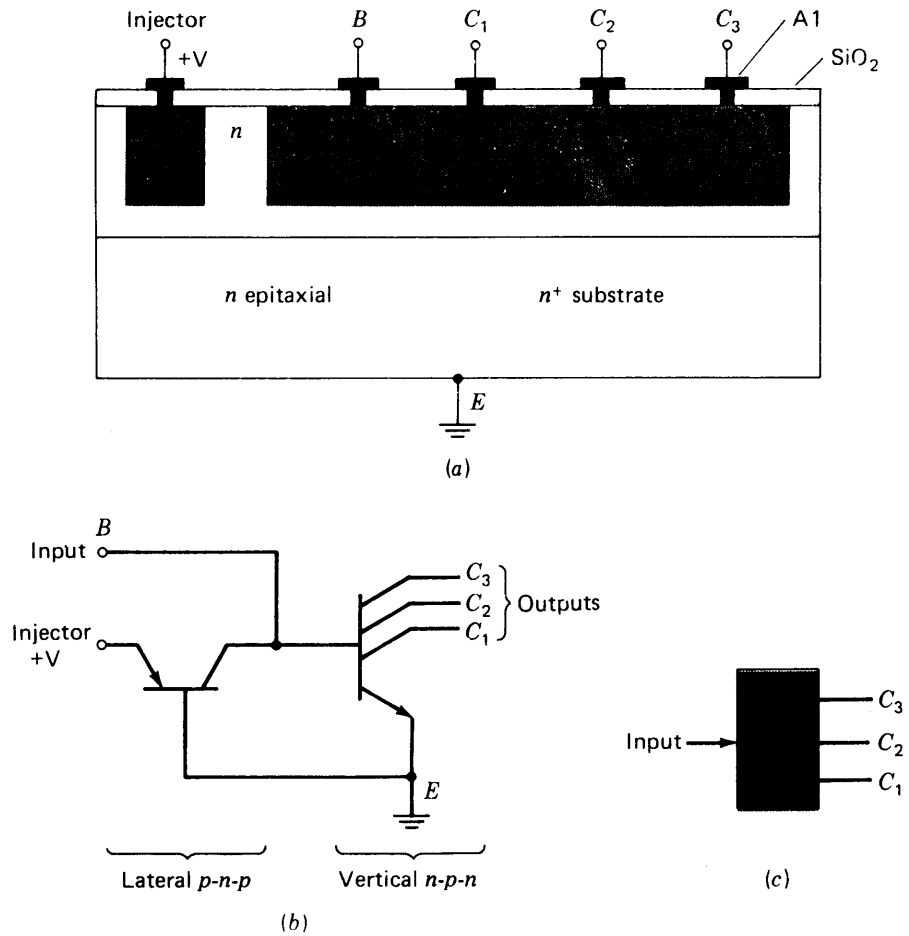| TABLE E.1							CIRCUIT LINE CHARACTERISTICS
	STANDARD TTL 74	LOW-POWER TTL	DTL	SCHOTTKY CLAMPED TTL	CMOS 5-V SUPPLY	CMOS 10-V SUPPLY	ECL

APPENDIX F
IIL CIRCUITS

Integrated injection logic (IIL, or I^2L) circuits represent an attempt to use bipolar junction transistor technology and still attain MOS transistor packing densities and low power consumption. Compared to MOS, the standard bipolar technology attains higher speeds but requires resistors; the transistors are larger, and an isolation diffusion is needed, which wastes space on the chip. To alleviate these problems, several designs have been made where the same transistor region is used as part of two or more devices. This technique is called *merging*, and IIL is the most used merged technology.

Figure F.1 shows the basic IIL gate and a possible semiconductor layout. Each gate requires an injector transistor to feed current into the base. Notice the single input and multiple outputs (one collector junction per output). This is a nonstandard logic configuration, and no ANSI or MIL standard symbol exists for this circuit, although standards work is progressing, Figure F.1(c) shows a symbol that is widely used now.

To show how gates can be formed from this configuration, which is basically an inverter with multiple outputs, Fig. F.2(a) shows a NOR gate made from two of the circuits in Fig. F.1. The IIL outputs are *open-collector* outputs, and so connecting them forms a wired AND. As a result, in Fig. F.2(a) the inputs A and B are first inverted and then wire-ANDed to form $\overline{A} \cdot \overline{B}$, which is the same function as a NOR gate yields.

Figure F.2(b) shows how IIL gates can be used to OR inputs. In this case several outputs are available, each with the value $A + B$.

Figure F.2(c) shows how a NAND gate can be made by using IIL gates. In

Injector B C_1 C_2 C_3 A1

+V SiO₂

n

n epitaxial n^+ substrate

E

(a)

B

Input

Injector
+V

C_3
C_2 } Outputs
C_1

E

Lateral p-n-p　　Vertical n-p-n

(b)

Input →

C_3
C_2
C_1

(c)

FIGURE F.1

IIL gate.

this case the inputs must be outputs from the IIL gates since these are wire-ANDed. Again, multiple outputs are available.

Because the basic IIL gate has a single input and multiple outputs, design does not proceed along regular lines. The advantages of this technology are sufficient to overcome this problem, and IIL microprocessors are now available, as are some high-speed memories. IIL does not lend itself to chip interconnection in the way that TTL does, however, and seems primarily suited for large-scale integration (like MOS).

$$\overline{A} \cdot \overline{B} = \overline{A + B}$$

(a)

$A + B$
$A + B$
$A + B$

(b)

From
other
gate
outputs

A

B
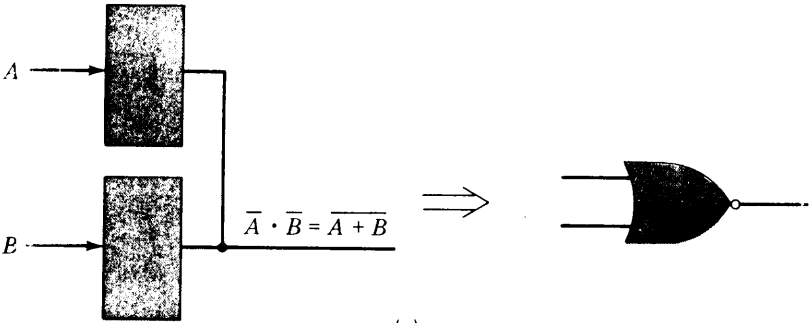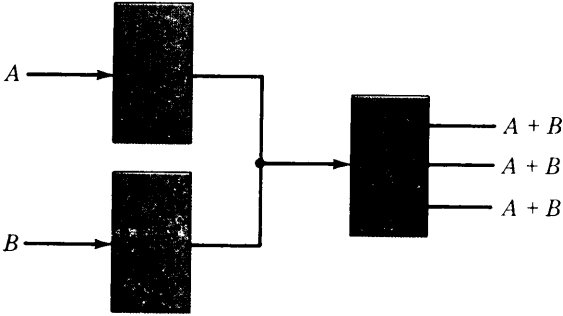
$\overline{A \cdot B}$
$\overline{A \cdot B}$
$\overline{A \cdot B}$
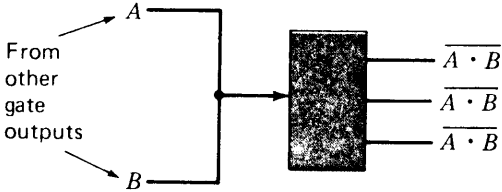
(c)

FIGURE F.2

IIL connections. (a) IIL
NOR gate function.
(b) IIL OR gate. (c) IIL
NAND gate function.

APPENDIX G
DAC IMPLEMENTATION

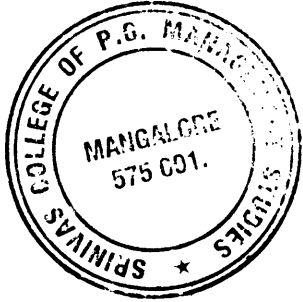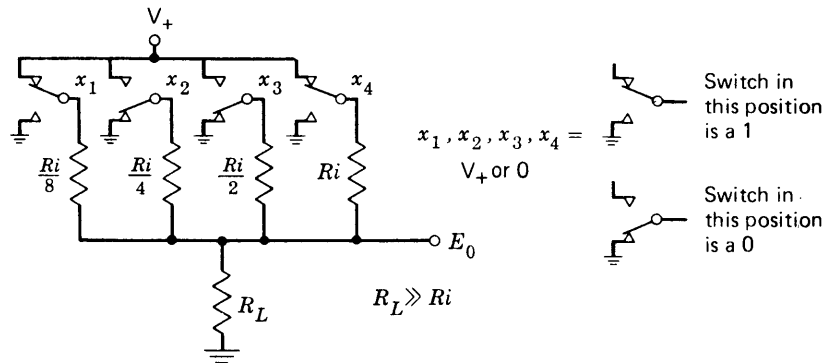The most straightforward digital-to-analog converter (DAC) involves the use of a resistor network. A basic type of resistor network DAC is illustrated in Fig. G.1, which shows a resistor network with four inputs. Each input is connected to a switch which connects a resistor to either 0 V or V_+. When a switch is in the position connecting to V_+, the binary bit represents a 1; when the switch connects to 0 V, the input bit is a binary 0. The output at E_0 will then be a dc voltage in the range of 0 to V_+ and will be proportional to the value of the binary number represented by the inputs.

For instance, if the input number is 0111 (leftmost switch down, other three up), the output voltage of E_0 will be $\frac{7}{15}V_+$; if the input is 1111, the output E_0 will be V_+; and if the input is 0001, the output E_0 will be at $\frac{1}{15}V_+$. For example, if V_+ were 15 V, then for an input of 0111 the output would be 7 V, for input 1000 the output would be 8, and for input 1111 (all switches up) the output would be 15 V. To achieve accuracy, all the resistors should be of the precision type. More resolution can be added by increasing the number of inputs and adding a resistor for each input. (The resistor values are halved for each input added.)

Resistor networks of this type are manufactured by several firms. The resistors are generally laser-beam-trimmed to the necessary accuracies. Often electronic (transistor-driven) switches are packaged in an IC container with the resistors, making a complete DAC.

Figure G.2 shows another type of resistor network which can be used for D/A conversion. The advantage of this network is that only two different values of resistors are used. The inputs are shown as switches, but generally semiconductor

V₊ or 0 — shown in figure

$x_1, x_2, x_3, x_4 = V_+ \text{ or } 0$

Switch in this position is a 1

Switch in this position is a 0

$R_L \gg Ri$

FIGURE G.1

D-to-A converter network.

Output

$2R$ R R R

$2R$ $2R$ $2R$ $2R$

LSB   MSB

+15 V
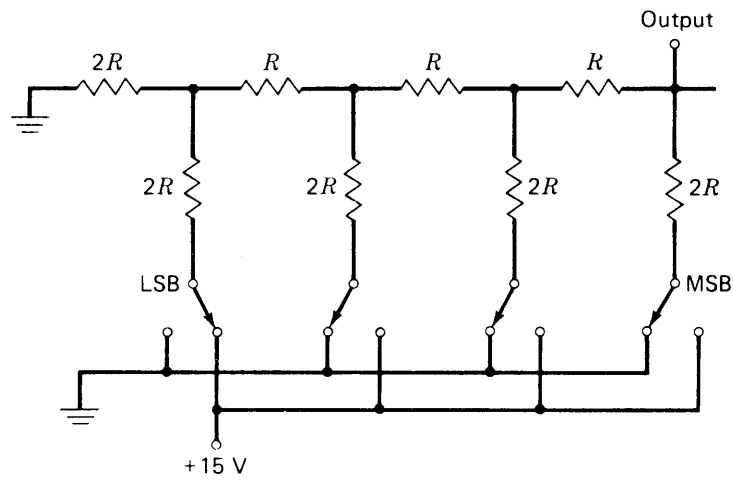
FIGURE G.2

D-to-A converter with two resistor sizes.

switches or level-setting amplifiers are used. The disadvantage of this converter is that two resistors are required per input.

There are several other circuits for DACs, and the design and construction of these devices represent a growing area in the computing field.

BIBLIOGRAPHY

Chapter 1

1 Grogano, P.: *Programming Pascal,* Addison-Wesley, Reading, MA, 1980.

2 Rauch-Hindin, W. B.: "Mainframes and Micros," *Systems and Software,* vol. 2, no. 6, June 1983.

3 Pier, K.: "A Retrospective on the Dorado, a High-Performance Personal Computer," *ACM 10th Annual Symposium on Computer Architecture, SIGARCH Newsletter,* vol. 11, no. 3, June 1983.

4 Welsh, J., and J. Elder: *Introduction to Pascal,* 2d ed., Prentice-Hall, Englewood Cliffs, NJ, 1982.

5 Clark, R., and S. Koehler: *The UCSD Pascal Handbook,* Prentice-Hall, Englewood Cliffs, NJ, 1982.

6 Tenenbaum, A. M., and M. J. Augenstein: *Data Structures Using Pascal,* Prentice-Hall, Englewood Cliffs, NJ, 1982.

Chapter 2

1 Rajeraman, V., and T. Radhakrishman: *Introduction to Digital Computer Design,* Prentice-Hall, Englewood Cliffs, NJ, 1983.

2 Iliff, S.: *Advanced Computer Design,* Prentice-Hall, Englewood Cliffs, NJ, 1982.

3 Bell, C. G., et al.: *Computer Engineering,* Digital Equipment Corp., Maynard, ME, 1976.

4   Hwang, K.: *Computer Arithmetic*, Wiley, New York, 1979.

5   Ong, S., and D. E. Atkins: "A Basis for the Quantitative Comparison of Computer Number Systems," *IEEE Trans. on Computers*, vol. C-32, no. 4, April 1983.

6   Kornerup, P., and D. W. Matula: "Finite Precision Rational Arithmetic," *IEEE Trans. on Computers*, vol. C-32, no. 4, April 1983.

Chapter 3

1   Parker, R., and S. Shapiro: "Workstations That Take the Chip's Design from End to End," *Computer Design*, vol. 22, no. 8, July 1980.

2   Agazzi, E.: *Modern Logic*, D. Reidel, Hingham, MA, 1980.

3   Marik, W., and Z. Onyszkiewicy: *Elements of Logic Foundations of Mathematics in Problems*, D. Reidel, Hingham, MA, 1982.

4   Fletcher, W. I.: *An Engineering Approach to Digital Design*, Prentice-Hall, Englewood Cliffs, NJ, 1980.

5   Bywater, R. E. H.: *Hardware/Software Design of Digital Systems*, Prentice-Hall, Englewood Cliffs, NJ, 1981.

6   Ramanatha, K. S., and N. N. Biswas: "A Design for Testability of Undetectable Crosspoint Faults in Programmable Logic Arrays," *IEEE Trans. on Computers*, vol. C-32, no. 6, June 1983.

Chapter 4

1   Bursky, D.: "New Processes, Device Structures Point to Million-Transistor IC," *Electronic Design*, vol. 31, no. 12, June 1983.

2   Fisher, A., and H. Kung: "Synchronizing Large VLSI Processor Arrays," *ACM 10th Annual Symposium on Computer Architecture, SIGARCH Newsletter*, vol. 11, no. 3, June 1983.

3   Kline, R.: *Structured Digital Design Including MSI/LSI Components and Microprocessors*, Prentice-Hall, Englewood Cliffs, NJ, 1983.

4   Marcus, M.: *Switching Circuits for Engineers*, Prentice-Hall, Englewood Cliffs, NJ, 1975.

5   McCurdy, L., and A. McHenry: *Digital Logic Design and Applications—An Experimental Approach*, Prentice-Hall, Englewood Cliffs, NJ, 1981.

6   *Integrated Fuse Logic Data Manual*, Signetics Corp., Sunnyvale, CA, 1983.

Chapter 5

1   Ling, J.: "High-Speed Binary Adder," *IBM Journal of Research and Development*, vol. 25, nos. 2 and 3, May 1981.

2   Hwang, K.: *Computer Arithmetic*, Wiley, New York, 1979.

3 "Floating Point ROM," Motorola Semiconductor MC68A39, Motorola Corp., Austin, TX, 1983.

4 Waser, S.: "High-Speed Monolithic Multipliers for Real-Time Digital Signal Processing," *Computer*, vol. 5, no. 6, October 1979.

5 Technical Staff of Monolithic Memories, Inc.: *Designing with Programmable Array Logic*, McGraw-Hill, New York, 1981.

6 Coonen, J. T.: "An Implementation Guide to a Proposed Standard for Floating Point Arithmetic," *Computer*, vol. 6, no. 7, Jan. 1980.

7 Parasuroman, B.: "Hardware Multiplication Techniques for Microprocessor Systems," *Computer Design*, vol. 18, no. 5, April 1977.

8 Watamuki, O., and M. D. Erreguvac: "Floating Point On-Line Arithmetic for Addition, Subtraction and Multiplication," *IEEE Trans. on Computers*, vol. C-32, no. 4, April 1983.

Chapter 6

1 McLeod, J.: "Data Storage Interface," *Systems and Software*, vol. 2, no. 6, June 1983.

2 Killman, P.: "Tiny Floppies Squeeze in the Bits," *Computer Design*, vol. 22, no. 6, 1983.

3 Domsky, L. D.: "Built for Speed: Quarter Inch Streaming Tape Drives," *Computer Design*, vol. 22, no. 1, May 1983.

4 Hemmerick, L. D.: "Rethinking Winchester Backups," *Computer Design*, vol. 22, no. 6, May 1983.

5 Jones, F., and A. Lancaster: "EEPROM Adapts Easily to System Change, *Electronics Design*, vol. 21, no. 17, Aug. 1983.

6 Pope, K.: "No Waiting—EEPROM at Work," *Computer Design*, vol. 22, no. 7, June 1983.

7 Bursky, D.: "Innovative Chips Designs Lead to Dense, Superfast RAMs," *Electronic Design*, vol. 21, no. 17, Aug. 1983.

8 Warren, C.: "Tape Unravels Secondary Storage Knots," *Electronic Design*, vol. 21, no. 17, Aug. 1983.

9 Ohr, S.: "Optical Disks Launching Gigabyte Data Storage," *Electronic Design*, vol. 21, no. 17, Aug. 1983.

10 Longfellow, D., and H. Sussman: "32 K-by-8 DRAM Reduces Size, Cost of Microprocessor Systems," *Electronic Design*, vol. 21, no. 17, Aug. 1983.

11 White, R. M.: "Magnetic Disks: Storage Densities on the Rise," *IEEE Spectrum*, vol. 20, no. 8, Aug. 1983.

12 Chi, C. S.: "Advances in Computer Mass Storage Technology," *Computer*, vol. 15, no. 5, May 1982.

ANSWERS TO SELECTED ODD-NUMBERED QUESTIONS

Chapter 1

1.7

ADDRESS	OP CODE	ADDRESS PART
1	CLA	40
2	ADD	41
3	ADD	42
4	STO	43
5	HLT	000
40	contains	X
41	contains	Y
42	contains	Z
43	contains	0

1.9

ADDRESS	OPERATION	OPERAND
1	CLA	20
2	MUL	20
3	STO	40
4	CLA	21
5	MUL	21
6	ADD	40
7	STO	40
8	CLA	22
9	MUL	22
10	ADD	40
11	STO	40
12	HLT	
20	contains	X
21	contains	Y
22	contains	Z
40	contains	0

1.13

ADDRESS	OPERATION	OPERAND
1	CLA	20
2	STO	21
3	CLA	21
4	MUL	20
5	STO	21
6	CLA	50
7	ADD	51
8	STO	50
9	BRM	3
10	CLA	21
11	ADD	20
12	STO	40
13	HLT	
20	contains	X
21	contains	0
50	contains	−5
51	contains	1

We will store our $X^5 + X$ in the address assigned by the assembler to the variable D.

ADDRESS	OPERATION	OPERAND
A	DEC	0
B	DEC	−5
C	DEC	1
D	DEC	0
	CLA	X
	STO	D
E	CLA	D
	MUL	X
	STO	D
	CLA	B
	ADD	C
	STO	B
	BRM	E
	CLA	D
	ADD	X
	STO	D
	HLT	

1.19

If we assume that the integers are in ascending or descending order only,

ADDRESS	OPERATION	OPERAND
1	CLA	30
2	SUB	31
3	BRM	5
4	HLT	
5	HLT	

The computer stops at address 4 if the numbers are in ascending order and at 5 if the numbers are in descending order. We must check to see whether the numbers are in ascending or descending order.

ADDRESS	OPERATION	OPERAND
1	CLA	30
2	SUB	31
3	BRM	10
4	CLA	31
5	SUB	32
6	BRM	13
7	HLT	
10	CLA	31
11	SUB	32
12	BRM	15
13	HLT	
15	HLT	

This program stops at address 13 if the numbers are in neither ascending nor descending order, at address 7 if the numbers are ascending, and at address 15 if the numbers are descending.

1.23

ADDRESS	OPERATION	OPERAND
1	CLA	26
2	SUB	25
3	BRM	300
4	BRA	400

1.25

ADDRESS	OPERATION	OPERAND
P	CLA	A
	SUB	B
	BRM	M
	CLA	A
	SUB	C
	BRM	M
	CLA	A
	STO	X
	HLT	
M	CLA	B
	SUB	C
	BRM	N
	CLA	B
	STO	X
	HLT	
N	CLA	C
	STO	X
	HLT	

1.32

ADDRESS	OPERATION	OPERAND	ADDRESS	OPERATION	OPERAND
1	CLA	300	13	CLA	6
2	BRM	5	14	ADD	400
3	STO	300	15	STO	6
4	BRA	7	16	CLA	401
5	SUB	300	17	ADD	400
6	SUB	300	18	STO	401
7	CLA	3	19	BRM	1
8	ADD	400	20	HLT	
9	STO	3	300⎫		
10	CLA	5	329⎭	contains numbers	
11	ADD	400	400	contains 1	
12	STO	5	401	contains −30	

Chapter 2

2.1 (*a*) 101011   (*b*) 1000000   (*c*) 100000000000   (*d*) 0.011
(*e*) 0.11011   (*f*) 0.0111   (*g*) 1000000000.1   (*h*) 10000011.1001
(*i*) 10000000000.0001

2.3 (*a*) 13   (*b*) 27   (*c*) 23   (*d*) 0.6875   (*e*) 0.203125   (*f*) 0.212890625
(*g*) 59.6875   (*h*) 91.203125   (*i*) 22.3408203125

2.5 (*a*) 11   (*b*) 36   (*c*) 19   (*d*) 0.8125   (*e*) 0.5625   (*f*) 0.3125
(*g*) 11.1875   (*h*) 9.5625   (*i*) 5.375

2.7 (*a*) 10100.11 = 20.75   (*b*) 1001010 = 74   (*c*) 1.1 = 1.5
(*d*) 10101 = 21

2.9 (*a*)

$$\begin{array}{ll} 1101.1 & 13.5 \\ \underline{1011.1} & \underline{11.5} \\ 11001.0 & 25 \end{array}$$

(*b*)

$$\begin{array}{ll} 101101 & 45 \\ \underline{110110} & \underline{109} \\ 1100011 & 154 \end{array}$$

(*c*)

$$\begin{array}{ll} 0.0011 & 0.1875 \\ \underline{0.1110} & \underline{0.875} \\ 1.0001 & 1.0625 \end{array}$$

(*d*)

$$\begin{array}{ll} 1100.011 & 12.375 \\ \underline{1011.011} & \underline{11.375} \\ 10111.110 & 23.750 \end{array}$$

2.11 (*a*)

$$\begin{array}{l} 1000000 \\ \underline{-100000} \\ 100000 \end{array}$$

(*b*)

$$\begin{array}{l} 1111111 \\ \underline{-111111} \\ 1000000 \end{array}$$

(*c*)

$$\begin{array}{l} 1011101.1 \\ \underline{-101010.11} \\ 110010.11 \end{array}$$

(*d*)

$$\begin{array}{l} 1010100.01001 \\ \underline{-110000.01010} \\ 100011.11111 \end{array}$$

2.13 (*a*)

$$\begin{array}{l} 100101 \\ \underline{-100011} \\ 000010 \end{array}$$

(*b*)

$$\begin{array}{l} 10000000 \\ \underline{01000000} \\ 1000000 \end{array}$$

(*c*)

$$\begin{array}{l} 1011110.1 \\ \underline{101011.11} \\ 110010.11 \end{array}$$

(*d*)

$$\begin{array}{l} 11111111 \\ \underline{1111111} \\ 10000000 \end{array}$$

2.15 (*a*) 100100000   (*b*) 11111100   (*c*) 100   (*d*) 1.1   (*e*) 10100000001.101
(*f*) 10.1

2.17 (a)
```
    1111
    1101
    1111
   11110
    1111
 11000011
```

(b)
```
    1111
    1010
   11110
   11110
 10010110
```

(c)
```
        100
 1011)101100
       1011
        000
```

(d)
```
         11.1
 1100)101010.0
       1100
      10010
       1100
       1100
       1100
          0
```

(e)
```
   111.11
    10.1
   11111
  111110
 10011.011
```

(f)
```
   10110.1
    100.11
   101101
   101101
  10110100
 1101010.111
```

2.19

	9s COMPLEMENT	10s COMPLEMENT
(a)	4563	4564
(b)	8067	8068
(c)	54.84	54.85
(d)	81.706	81.707

2.21

	9s COMPLEMENT	10s COMPLEMENT
(a)	6345	6346
(b)	7877	7878
(c)	45.80	45.81
(d)	62.736	62.737

2.23

	1s COMPLEMENT	2s COMPLEMENT
(a)	0100	0101
(b)	00100	00101
(c)	0100.10	0100.11
(d)	00100.10	00100.11

2.25

	1s COMPLEMENT	2s COMPLEMENT
(a)	010000	010001
(b)	011011	011100
(c)	01000.01	01000.10
(d)	01100.00	

2.27

	9s COMPLEMENT	10s COMPLEMENT
(a)	948	948

9s COMPLEMENT:
```
    948
    765
  1 713
   └→ 1
    714
```

10s COMPLEMENT:
```
  948
  766
  714
```

(b)   347   347
        736   737
      1 083   084
        └→ 1
        084

(c)   349.5   349.5
       754.6   754.7
     1 104.1   104.2
       └→ 1
       104.2

(d)   412.7   412.7
       590.7   590.8
     1 003.4   3.5
       └→ 1
         3.5

2.29   9s COMPLEMENT   10s COMPLEMENT
(a)   1024   1024
             9086   9087
           ┌ 0110   0111
           └→ 1
             111

(b)   249   249
             862   863
           ┌ 111   112
           └→ 1
             112

(c)   24.1   24.1
             86.5   86.6
           ┌ 10.6   10.7
           └→ 1
             10.7

(d)   239.3   239.3
             880.5   880.6
           ┌ 119.8   119.9
           └→ 1
             119.9

2.31   1s COMPLEMENT   2s COMPLEMENT
(a)   1011   1011
             1010   1011
           1 0101   0110
             └→ 1
             0110

(b)   11011   11011
             00110   00111
           1 00001   00010
             └→ 1
             10

(c)
```
    10111.1        10111.1
    01100.0        01100.1
  1 00011.1         100.0
  └──────→ 1
    100.0
```

(d)
```
    11011.00       11011.00
    01100.00       01100.01
  1 00111.00        111.01
  └──────→ 1
    111.01
```

2.33 $2^6 = 64$

2.35 1000 different numbers in each case (from 0 to 999, for instance)

2.37 0, 1, 2, 3, 10, 11, 12, 13, 20, 21

2.39 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 20, 21, 22

2.41

(a)
```
    .1001
    .1001
  ┌ 0010
  └──→ 1
    .0011
```

(b)
```
    .1110
    .1001
  ┌ 0111
  └──→ 1
    .1000
```

(c)
```
    01111
    10110
  ┌ 00101
  └──→ 1
    .00110
```

(d)
```
    11011
    00110
  ┌ 00001
  └──→ 1
    00010
```

(e)
```
    1110101
    0101101
  1 0100010
  └──────→ 1
    0100011
```

2.45

(a)
```
    45,056
     1,536
       192
         7
    46,791
```

(b)
```
    24,576
     1,024
       160
        12
    25,772
```

(c)
```
    40,960
     1,024
       144
         2
    42,130
```

(d)
```
    851,968
      8,192
      1,792
         96
          3
    862,051
```

2.49 (a) 55 (b) 556 (c) 267 (d) 66.3 (e) 3.554

2.53 (a) 1644. (b) 514 (c) 1041.3 (d) 1170.76051 (e) 10515.5

2.57 (a) B7 (b) 9C (c) 5F (d) 0.7E (e) B7A

2.61

(a)
```
       1
      15₈
    + 14₈
      31₈
```

(b)
```
       1
      24₈
    + 36₈
      62₈
```

(c)
```
       1
     126₈
     347₈
     475₈
```

(d)
```
      1
     67₈
     45₈
    134₈
```

(e)
```
       1
     136₈
     636₈
     774₈
```

3.1

(a)

X	Y	Z	XYZ	$X\overline{Y}\overline{Z}$	$XYZ + X\overline{Y}\overline{Z}$
0	0	0	0	1	1
0	0	1	0	0	0
0	1	0	0	0	0
0	1	1	0	0	0
1	0	0	0	0	0
1	0	1	0	0	0
1	1	0	0	0	0
1	1	1	1	0	1

(b)

A	B	C	ABC	$A\overline{B}\overline{C}$	$\overline{A}\overline{B}\overline{C}$	$ABC + A\overline{B}\overline{C} + \overline{A}\overline{B}\overline{C}$
0	0	0	0	0	1	1
0	0	1	0	0	0	0
0	1	0	0	0	0	0
0	1	1	0	0	0	0
1	0	0	0	1	0	1
1	0	1	0	0	0	0
1	1	0	0	0	0	0
1	1	1	1	0	0	1

(c)

A	B	C	$B\overline{C}$	$\overline{B}C$	$B\overline{C} + \overline{B}C$	$A(B\overline{C} + \overline{B}C)$
0	0	0	0	0	0	0
0	0	1	0	1	1	0
0	1	0	1	0	1	0
0	1	1	0	0	0	0
1	0	0	0	0	0	0
1	0	1	0	1	1	1
1	1	0	1	0	1	1
1	1	1	0	0	0	0

(d)

A	B	C	$A + B$	$A + C$	$\overline{A} + \overline{B}$	$(A + B)(A + C)(\overline{A} + \overline{B})$
0	0	0	0	0	1	0
0	0	1	0	1	1	0
0	1	0	1	0	1	0
0	1	1	1	1	1	1
1	0	0	1	1	1	1
1	0	1	1	1	1	1
1	1	0	1	1	0	0
1	1	1	1	1	0	0

3.3 Only the values of the expressions are listed:

(a)

A	B	$A\overline{B} + \overline{A}B$
0	0	0
0	1	1
1	0	1
1	1	0

(b)

A	B	C	$A\bar{B} + B\bar{C}$
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

(c)

A	C	$A\bar{C} + AC$
0	0	0
0	1	0
1	0	1
1	1	1

(d)

A	B	C	$A\bar{B}C + AB\bar{C} + \bar{A}BC$
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

(e)

A	B	C	$A(\bar{A}BC + A\bar{B}C + AB\bar{C})$
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

3.7   (a) $\bar{B}C + \bar{A}C + \bar{A}B$ (b) $\bar{C} + \bar{B} + \bar{A}$

      (c) $A(B + C)$ (d) A is a minimal expression

3.9   (a) $ABC(A\bar{B}\bar{C} + \bar{A}BC + \bar{A}B\bar{C}) = 0$, for no assignment of binary values will make this expression take the value 0.

      (b) $AB + A\bar{B} + \bar{A}C + \bar{A}\bar{C} = 1$, for every assignment of values will give this expression the value 1.

      (c) $XY + XYZ + XY\bar{Z} + \bar{X}YZ = XY + YZ$

      (d) $XY(\bar{X}YZ + X\bar{Y}Z + \bar{X}\bar{Y}\bar{Z}) = 0$

3.11   (a) $\bar{A}(\bar{B} + \bar{C})(\bar{A} + \bar{B}) = \bar{A}B + \bar{A}C$ or $\bar{A}(\bar{B} + \bar{C})$

       (b) $\bar{A}B + \bar{B}C + \bar{A}C$

(c) $(\bar{A} + \bar{B})(B + \bar{C})(\bar{C} + D) = \overline{AB}\bar{C} + \bar{A}\bar{C} + \bar{A}BD + \bar{A}\bar{C}D$
$$= \bar{A}\bar{C} + \bar{B}\bar{C} + \bar{A}BD$$

(d) $(\bar{A} + \bar{B}) + (C + \bar{D})(B + \bar{C}) = \bar{A} + \bar{B} + BC + B\bar{D} + \overline{CD}$
$$= \overline{AB} + C + \bar{D}$$

(e) $\bar{A} + \overline{BC} + CD$

3.13 The important columns in these tables are as follows:

X	Y	Z	$(\overline{X + Y + Z})$	$\overline{X}\overline{Y}\overline{Z}$
0	0	0	1	1
0	0	1	0	0
0	1	0	0	0
0	1	1	0	0
1	0	0	0	0
1	0	1	0	0
1	1	0	0	0
1	1	1	0	0

X	Y	Z	$(\overline{XYZ})$	$\bar{X} + \bar{Y} + \bar{Z}$
0	0	0	1	1
0	0	1	1	1
0	1	0	1	1
0	1	1	1	1
1	0	0	1	1
1	0	1	1	1
1	1	0	1	1
1	1	1	0	0

3.15 (a) $\bar{A}BC + A\bar{B}C + AC + BC = AC + BC$

(b) $A\bar{B} + A\bar{C} + ABC + AB\bar{C} + \bar{A}BC + \bar{B}C$ (This can be simplified to $\bar{B}C$)

(c) $A\bar{B} + A\bar{B}C = A\bar{B}$

3.17 Rule 13

3.19 (a) $AB + AD + BC + CD$

(b) $AB + AD + AC + BC + CD + C + BD + D + DC = C + D + AB$

(c) $ABC + ABD + AC + BC + DC + ADC + BDC + DC = AC + BC + DC + ABD$

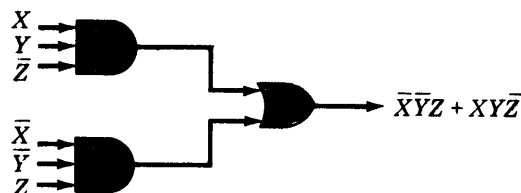(d) $A\bar{B} + A\bar{C}$

3.21 $\overline{X}\overline{Y}Z + XY\overline{Z}$

3.25 $XY + X\bar{Z}$ **591**

ANSWERS TC
SELECTED
ODD-NUMBERED
QUESTIONS

FIGURE A3.25

3.25 $XY + X\bar{Z}$
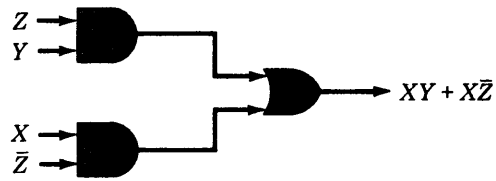
FIGURE A3.25

3.27

X	Y	$X + \bar{X}Y$	$X + Y$
0	0	0	0
0	1	1	1
1	0	1	1
1	1	1	1

3.29 $Y\bar{Z} + \bar{Y}Z$ is the sum-of-products expression, and $(Y + Z)(\bar{Y} + \bar{Z})$ is the product-of-sums expression.

3.35 (a)

	$\bar{X}$	X
$\bar{Y}$	1	
Y	1	

$\bar{X}\bar{Y} + \bar{X}Y$

(b)

	$\bar{X}\bar{Y}$	$\bar{X}Y$	XY	$X\bar{Y}$
$\bar{Z}$	1		1	
Z				

$\bar{X}\bar{Y}\bar{Z} + XY\bar{Z}$

(c)

	$\bar{X}\bar{Y}$	$\bar{X}Y$	XY	$X\bar{Y}$
$\bar{Z}$	1	1		
Z	1			

$\bar{X}\bar{Y}\bar{Z} + \bar{X}Y$

(d)

	$\bar{X}\bar{Y}$	$\bar{X}Y$	XY	$X\bar{Y}$
$\bar{Z}$	1	1		1
Z				

$\bar{X}\bar{Y}\bar{Z} + \bar{X}Y\bar{Z} + X\bar{Y}\bar{Z}$

(e)

	$\bar{X}\bar{Y}$	XY	XY	$X\bar{Y}$
$\bar{Z}$	1	1		1
Z				

$\bar{X}\bar{Z} + \bar{Y}\bar{Z}$

(f)

	$\bar{A}\bar{B}$	$\bar{A}B$	AB	$A\bar{B}$
C				
C				

$AB(\bar{A}\bar{B}\bar{C} + \bar{B}C)$

3.39 (a)

	$\bar{X}$	X
$\bar{Y}$	1	1
Y		

$$X\bar{Y} + \bar{X}Y$$

(b)

	$\bar{A}\bar{B}$	$\bar{A}B$	AB	$A\bar{B}$
$\bar{C}$	1			1
C				

$$\bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C}$$

(c)

	$\bar{A}\bar{B}$	$\bar{A}B$	AB	$A\bar{B}$
$\bar{C}$				
C			1	1

$$AB C + AB\bar{C}$$

(d)

	$\bar{A}\bar{B}$	$\bar{A}B$	AB	$A\bar{B}$
$\bar{C}$			1	1
C			1	1

$$ABC + A\bar{B}\bar{C} + AB\bar{C} + ABC$$

(e)

	$\bar{A}\bar{B}$	$\bar{A}B$	AB	$A\bar{B}$
C				1
C			1	1

$$ABC + A\bar{B}\bar{C} + A\bar{B}C$$

(f)

	$\bar{A}\bar{B}$	$\bar{A}B$	AB	$A\bar{B}$
$\bar{C}$	1			
C		1	1	

$$ABC + \bar{A}BC + \bar{A}\bar{B}\bar{C}$$

3.41 (a)

	$\bar{X}\bar{Y}$	$\bar{X}Y$	XY	$X\bar{Y}$
$\bar{Z}$	1			
Z	1		1	1

$$m_0 + m_1 + m_5 + m_7$$

(b)

	$\bar{X}\bar{Y}$	$\bar{X}Y$	XY	$X\bar{Y}$
Z				1
Z	1	1		1

$$m_1 + m_3 + m_4 + m_5$$

(c)

	$\bar{X}\bar{Y}$	$\bar{X}Y$	XY	$X\bar{Y}$
$\bar{Z}$		1		
Z	1	1		1

$$m_1 + m_2 + m_3 + m_5$$

(d)

	$\overline{X}\overline{Y}$	$\overline{X}Y$	XY	$X\overline{Y}$
$\overline{Z}$	1			
Z			1	1

$$m_0 + m_5 + m_7$$

3.45 (b)

	$\overline{W}\overline{X}$	$\overline{W}X$	WX	$W\overline{X}$
$\overline{Y}\overline{Z}$	1	1	1	1
$\overline{Y}Z$			1	1
YZ				1
$Y\overline{Z}$	1			1

$m_0 = \overline{W}\overline{X}\overline{Y}\overline{Z}$ $m_{10} = W\overline{X}Y\overline{Z}$
$m_2 = \overline{W}\overline{X}Y\overline{Z}$ $m_{11} = W\overline{X}YZ$
$m_4 = \overline{W}X\overline{Y}\overline{Z}$ $m_{12} = WX\overline{Y}\overline{Z}$
$m_8 = W\overline{X}\overline{Y}\overline{Z}$ $m_{13} = WX\overline{Y}Z$
$m_9 = W\overline{X}\overline{Y}Z$

$m_0 + m_2 + m_4 + m_8 + m_9 + m_{10} + m_{11} + m_{12} + m_{13}$
$\overline{X}\overline{Z} + \overline{Y}\overline{Z} + W\overline{X} + W\overline{Y}$
$\overline{Z}(\overline{X} + \overline{Y}) + W(\overline{X} + \overline{Y})$
$(\overline{Z} + W)(\overline{X} + \overline{Y})$

3.47 (a) $m_1 + m_3 + m_5 + m_7 + m_{12} + m_{13} + m_8 + m_9$

	WX	$W\overline{X}$	$\overline{W}\overline{X}$	$\overline{W}X$
YZ	0	0	m_3	m_7
$Y\overline{Z}$	0	0	0	0
$\overline{Y}\overline{Z}$	m_{12}	m_8	0	0
$\overline{Y}Z$	m_{13}	m_0	m_1	m_5

Product of sums:

$$\overline{(WY + WZ)} = (\overline{W} + \overline{Y})(W + Z)$$

Sum of products:
$$W\overline{Y} + \overline{W}Z$$

(b) $m_0 + m_5 + m_7 + m_8 + m_{11} + m_{13} + m_{15}$

	WX	$W\overline{X}$	$\overline{W}\overline{X}$	$\overline{W}X$
YZ	m_{15}	m_{11}		m_7
$Y\overline{Z}$	0			0
$\overline{Y}\overline{Z}$	0	m_8	m_0	0
$\overline{Y}Z$	m_{13}			m_5

Product of sums:

$(X\overline{Z} + \overline{Y}\overline{Z} + \overline{W}\overline{X}Z + \overline{X}\overline{Y}Z)$
$= (\overline{X} + Z)(\overline{Y} + Z)(W + X + \overline{Z})$
$(X + Y + \overline{Z})$

3.49 (a) $\overline{A}\overline{B}\overline{C} + A\overline{B}\overline{C} + \overline{ABC} + \overline{A}B\overline{C} + \overline{A}\overline{B}C = \overline{B}\overline{C}$
(with don't-cares over $ABC + \overline{A}B\overline{C} + \overline{A}\overline{B}C$)

	AB	$A\overline{B}$	$\overline{A}\overline{B}$	$\overline{A}B$
$\overline{C}$	D		D	
C		1	1	D

(b) $ABC + A\overline{B}\overline{C} + \overline{AB}\overline{C} + A\overline{B}C = A$
(with don't-cares)

	AB	$A\overline{B}$	$\overline{A}\overline{B}$	$\overline{A}B$
C	1	D		
$\overline{C}$	D	1		

don't-cares

(c) $ABCD + \overline{A}\overline{B}\overline{C}D + \overline{A}BCD + \overline{A}\overline{B}CD + \overline{A}\overline{B}\overline{C}D + ABC\overline{D}$

	AB	$A\overline{B}$	$\overline{A}\overline{B}$	$\overline{A}B$	
CD	1	D	D	1	$CD + \overline{A}BD$
$C\overline{D}$	D				
$\overline{C}\overline{D}$					
$\overline{C}D$			1		

Chapter 4

4.1
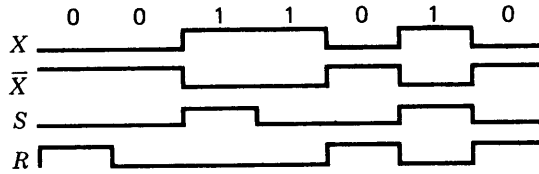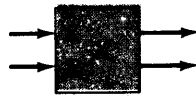
FIGURE A4.1

4.5

FIGURE A4.5

4.9
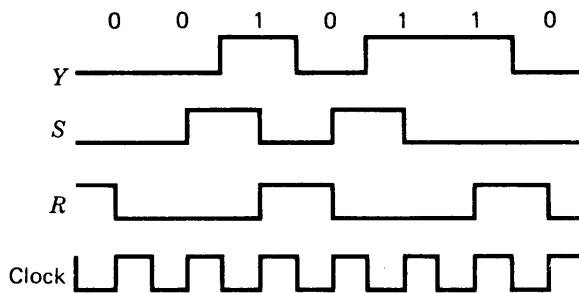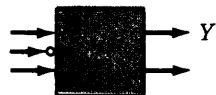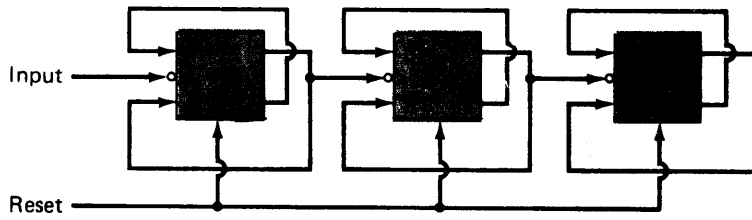
FIGURE A4.9

4.13
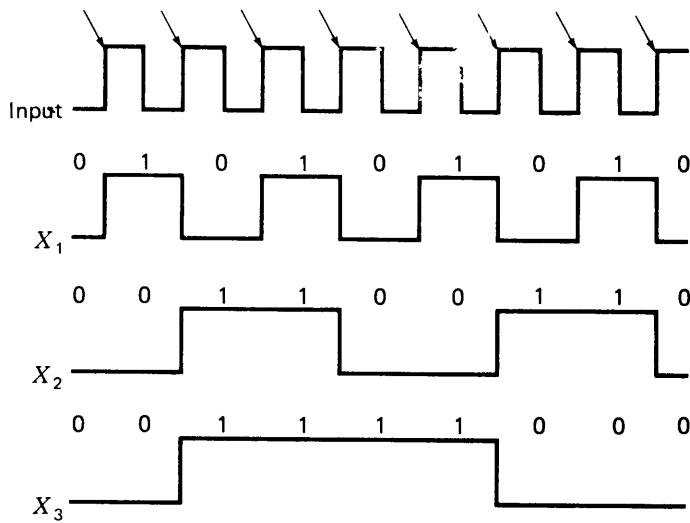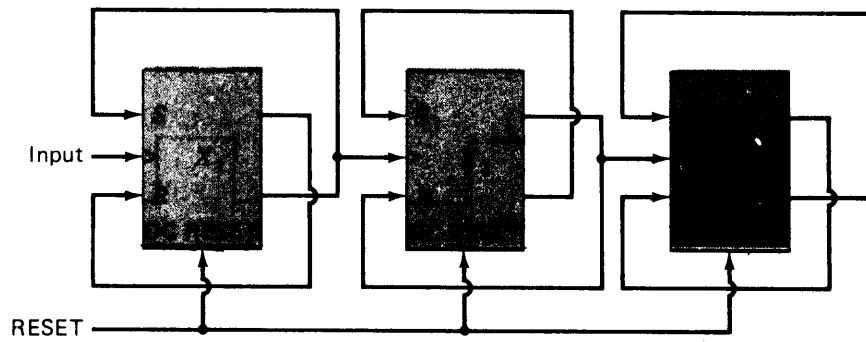
FIGURE A4.13
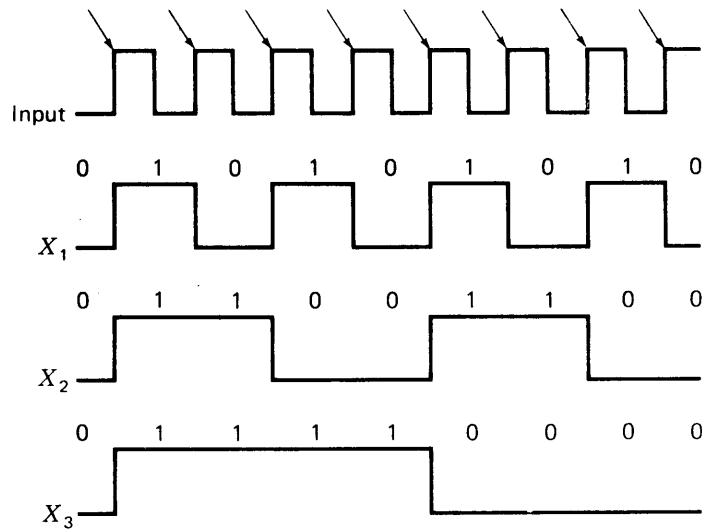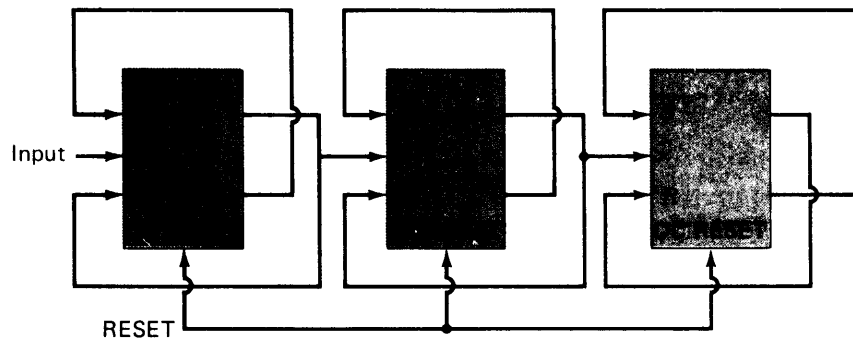
4.15

4.17

597

ANSWERS TO
SELECTED
ODD-NUMBERED
QUESTIONS
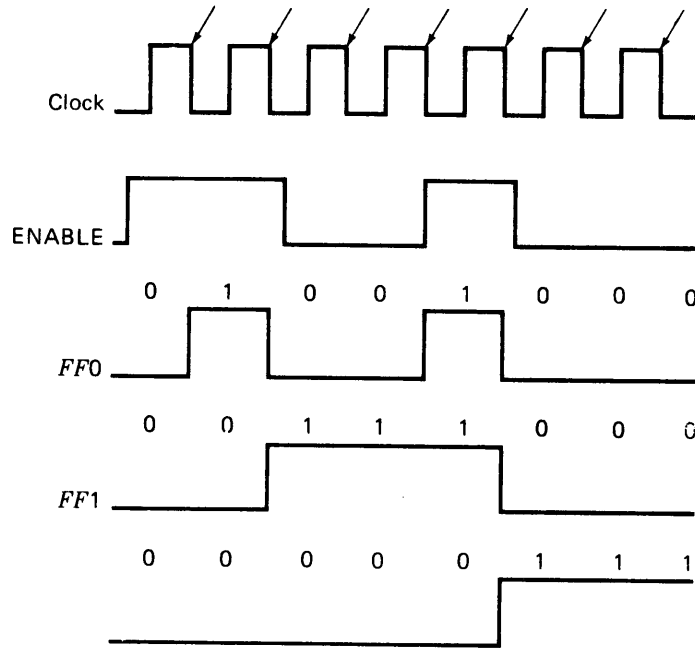
FIGURE A4.17

Chapter 5

5.1

FIGURE A5.1

1 for Y

1 for Y's 1s complement

Clock
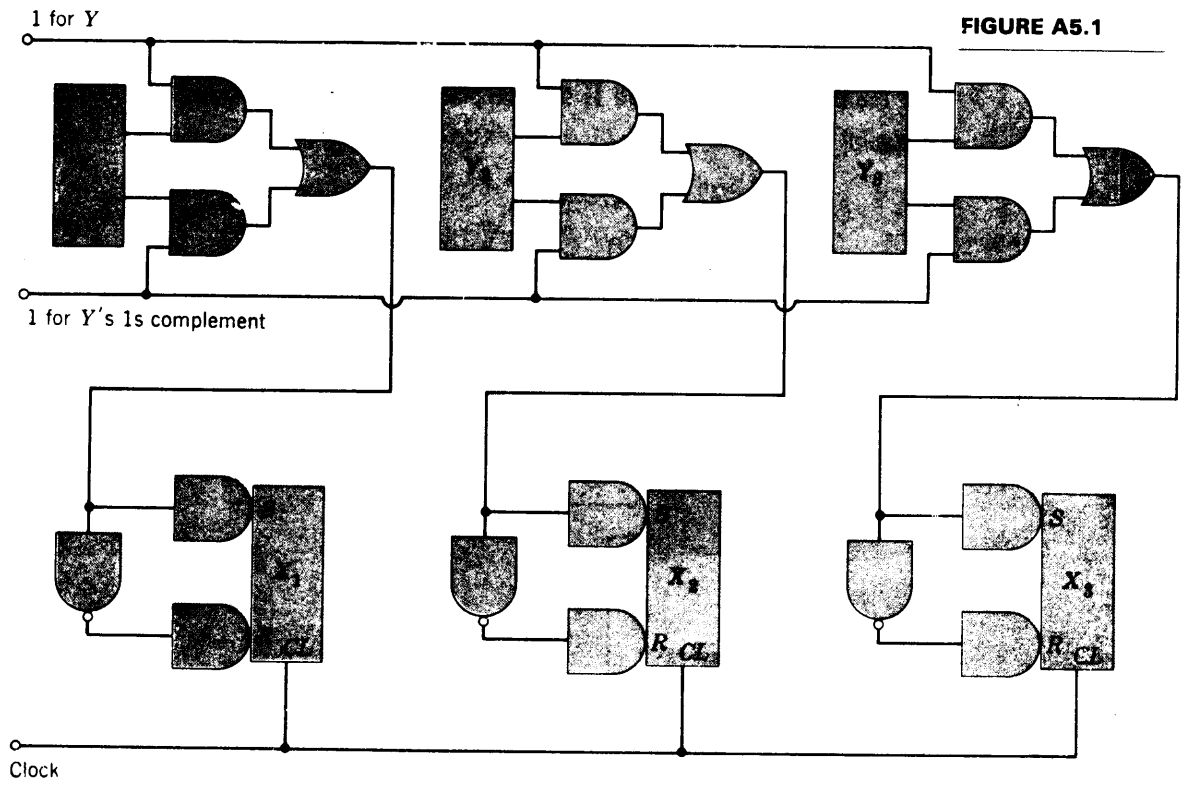
5.3   (a) $\underline{0}0110$ (b) $\underline{0}1010$ (c) $\underline{1}1100$ (d) Not representable

5.5 -4 would be stored $\underline{1}0100$ in the magnitude system, $\underline{1}1011$ in the 1s complement system, and $\underline{1}1100$ in the 2s complement system.

5.7 $S = 1$ and $C = 1$

5.9 -12 in 1s complement; -13 in 2s complement

5.11   The sum will overflow the register and cause an incorrect addition. Most machines sense for this and turn on an "addition overflow" or indicate the overflow in some manner.
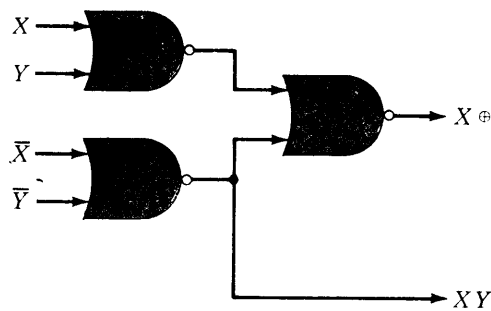
5.15

5.29   Logical addition, $\underline{0}111011$
Logical multiplication, $\underline{0}100010$
Exclusive OR, $\underline{0}011001$

5.31   The logical MULTIPLY will clear those digits of X where 0s occur in Y, and the logical ADD will add 1s into the places in X where 1s occur in Y.
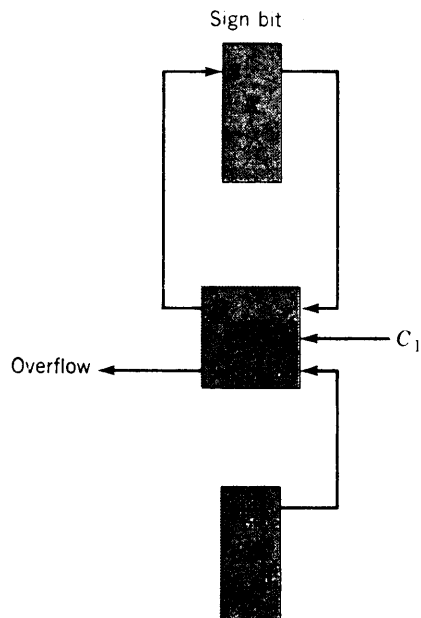
5.48

Overflow $= (X > \emptyset)\cdot(Y > \emptyset)\cdot(C_3 = 1) + (X < \emptyset)\cdot(Y < 0)\cdot(C_3 = \emptyset)$

Overflow $= \overline{X}_4\overline{Y}_4C_3 + X_4Y_4\overline{C}_3$

5.50 The general scheme is

Carry out = 1
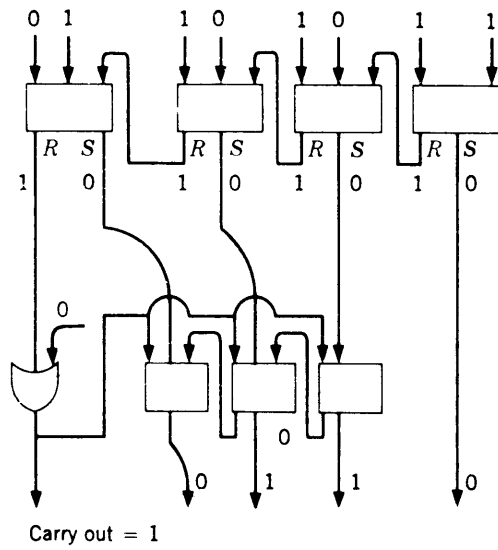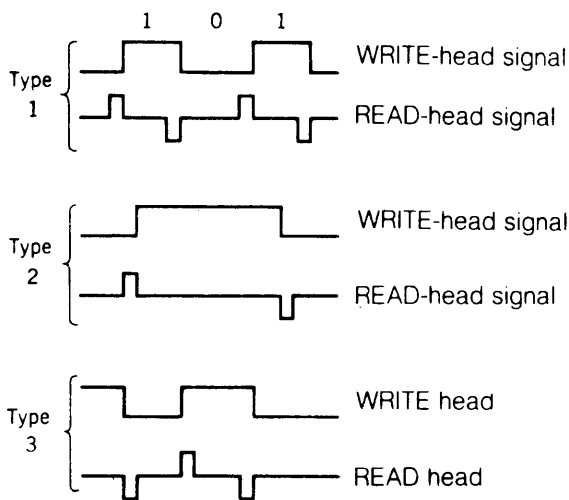
Chapter 6

6.12

6.35 262,500 bits/s

Chapter 7

7.3 01100001
01100100
01100100
00010000
00010110
00000100
00000001
10000000 Carriage return is optional

7.5 27 holes in three cards. Easier to correct if cards are used, for erroneous cards may simply be replaced.

7.7 Nine holes

7.9

DECIMAL	EXCESS-3 CODE	EVEN-PARITY CHECK	ODD-PARITY CHECK
0	0011	0	1
1	0100	1	0
2	0101	0	1
3	0110	0	1
4	0111	1	0
5	1000	1	0
6	1001	0	1
7	1010	0	1
8	1011	1	0
9	1100	0	1

7.11 (a) The errors are in the seventh, eighth, and ninth rows; the sixth digit in each row is in error, and the message is, "That's right."
(b) The error is the fourth digit in the sixth row, and the message is, "Don't stop."

7.13 10. One such code can be formed by adding a leading 0 to each of the four-binary-digit Gray code groups listed in Chap. 8 and then adding another 16 rows with the four rightmost binary digits the same as those in Chap. 8 but with their order reversed and with a leading 1 added to each code row.

7.15 (a) Errors are in the second, third, and fourth rows, the seventh digit in. The message is, "That's fine."
(b) Errors are in the second and third rows, the third digit in, and the message is, "Bad tapes." Notice that we corrected a double error in a column.

Chapter 8

8.16 To interface a keyboard with device address 6, modify Fig. 8.20 as follows. The keyboard-to-bus data line drivers remain the same and are not shown here. The address line selection logic is changed:
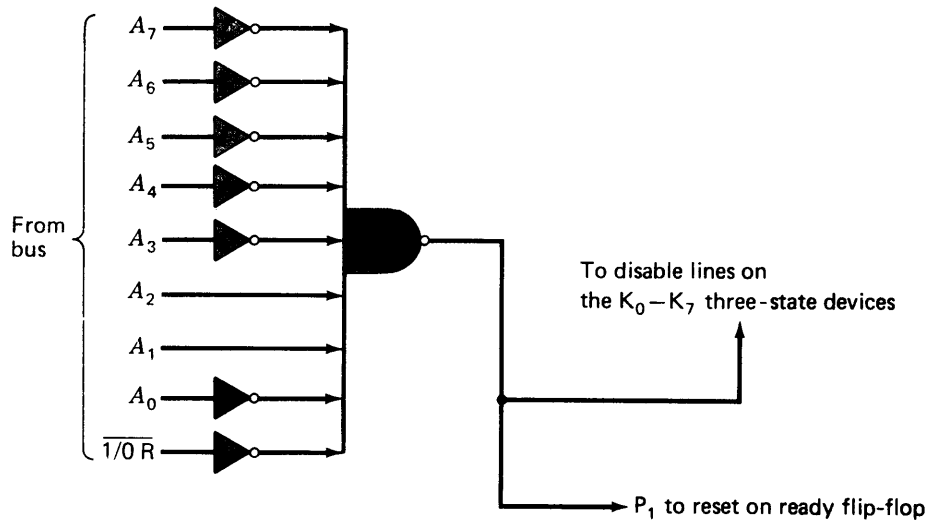
FIGURE A8.16

Chapter 9

9.3 The timing table is shown in Table 9.3 with the following additions:
OPCODE 00100 = BRM

BRM (from Table 9.4)

I and T_0	Set R	Tell memory to read instruction word
I and T_1	MB into OP,	Operation portion of instruction word into the operation register.
	RESET R	Clear memory read flip-flop.
I and T_2 and AC_0	MB into IC	If sign bit of accumulator is 1 (contents as negative), then use the address portion of the instruction address as the next instruction address.
I and T_2 and AC_0	INCREMENT IC	If sign bit of accumulator is 0 (contents are not negative), then use the next sequential address in memory as the next instruction address
I and T_3	IC INTO MA	Set up to read the next instruction from memory. Leave I = 1 so that the next cycle will be another instruction cycle.

BRA

I and T_0	SET R	Tell memory to read instruction
I and T_1	MB INTO OP,	Operation portion of instruction word into the operation register.
	RESET R	Clear memory read flip-flop.
I and T_2	MB INTO IC	Use address portion of instruction word as the next instruction address.
I and T_3	IC INTO MA	Set up to read the next instruction from memory. Leave I = 1 so that the next cycle will be another instruction cycle.
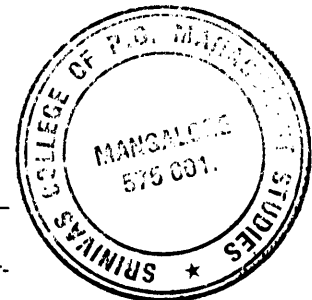
The control signal generation logic in Figs. 9.6 and 9.8 should be augmented with the following:
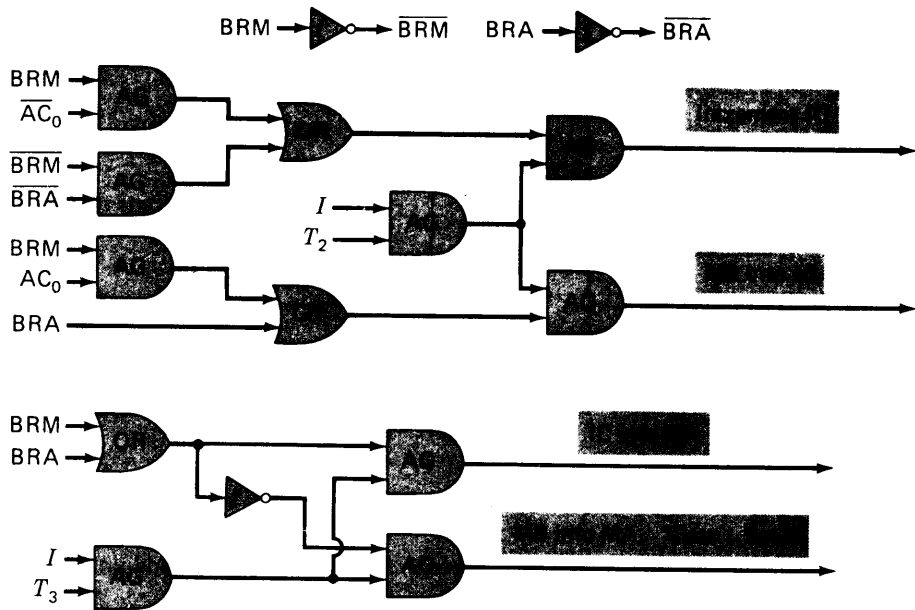

FIGURE A9.3

9.8 Instructions which require an execution cycle generally must access memory to obtain or to store an operand. Examples from the instruction set of Table 9.3 include ADD and STORE. Instructions which do not require an access to memory for an operand generally do not require an execution cycle. In such cases there may be no operand; or the operand has been obtained as part of the instruction and is manipulated solely within the central registers of the processor. Examples are BRM, BRA, and CLR.

9.18 This question says: Provide a microprogram for the BRM branch-on-minus instruction of Table 9.4. The OP code in the BRM instruction is $00100 = 4_{10}$.

MICROPROGRAM ROM LOCATION	C_0 to C_6	MICROPROGRAM C_7 to C_n
0	—	$1 \rightarrow R$; IAR + 1 $\rightarrow$ IAR
1	—	$MB_{0-4} \rightarrow OP$; IAR + 1 $\rightarrow$ IAR; 0 $\rightarrow$ R
2	—	OP + IAR + 1 $\rightarrow$ IAR
3	20_{10}	$C_{0-6} \rightarrow$ IAR
.	.	.
.	.	.
.	.	.
7	40_{10}	$C_{0-6} \rightarrow$ IAR
.	.	.
.	.	.
40	42_{10}	IF $(AC_0 = 1)$ THEN $C_{0-6} \rightarrow$ IAR; ELSE IAR + 1 $\rightarrow$ IAR
41	43_{10}	$C_{0-6} \rightarrow$ IAR; IC + 1 $\rightarrow$ IC
42	—	$MB_{0-24} \rightarrow$ IC
43	—	IC $\rightarrow$ MA; 0 $\rightarrow$ IAR
.	.	.
.	.	.
.	.	.